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42	BOM

IH11N-MHS H110MG PRO D4 VER 6.1

CPU:

Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:

SPT-H PCH

Main Memory:

Dual Channel/DDR-4*2(Max 16GB)1867/2133

Onboard Device:

Super I/O:IT8613E

LAN:Realtek 8111H

HD Codec:ALC887

Power solution:

CPU Voltage Regulators:3phase by RT3606

high 1 Low 1 OV by RT3606

DDR Voltage Regulators:1Phase by UP1514

high 1 Low 1 OV by IT8613E

Expansion Slots:

PCI EXPRESS 16X SLOT *1

PCI EXPRESS 1X SLOT *2

REAR IO:

PS/2 PORT

DVI Port

VGA Port

USB3.0 PORT *2

Gb RJ-45 +2 layer USB3.0 Ports

Audio Jackets (3 PORT)

Front I/O:

SATA3 *6

USB 2.0 Header * 2

Serial header


USB 3.0 Header * 1

Front Audio Header

CPU FAN *1

System FAN *1

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2.VER0.60:COLAY REMOVE VGT_PH2(PAGE39)

3.VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)

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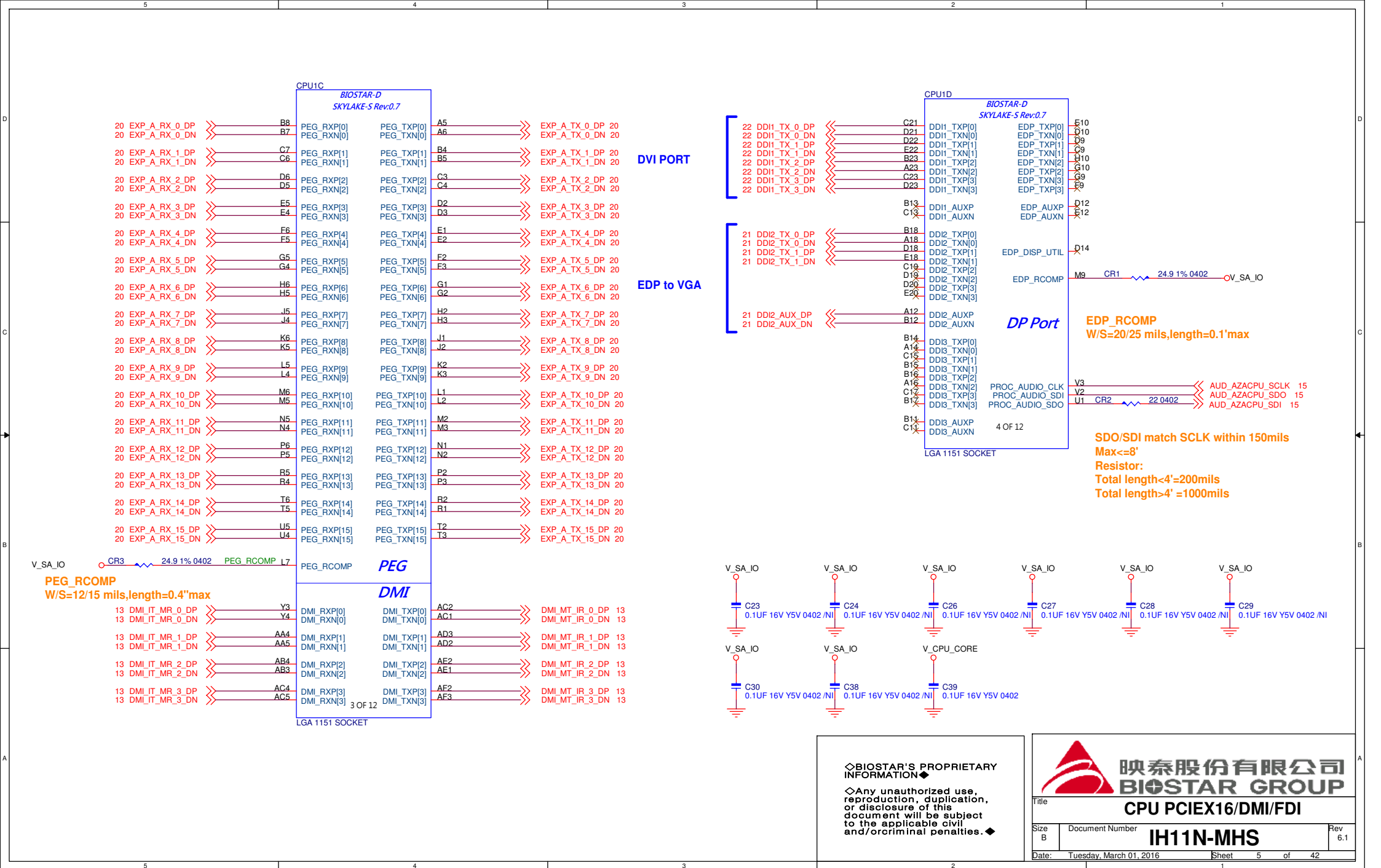


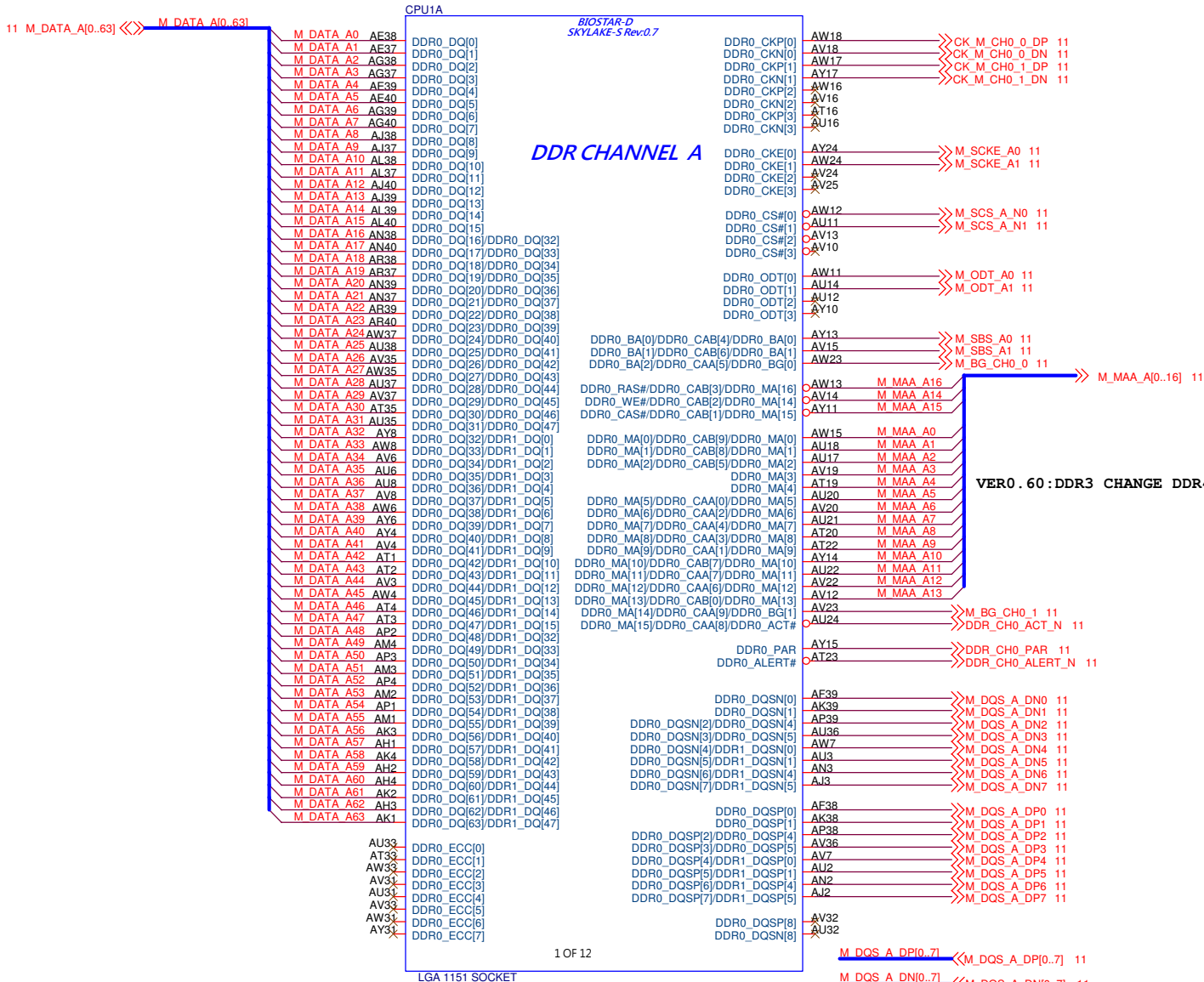
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Title CPU PCIEX16/DMI/FDI

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Title CPU DDR3 CHANNEL A

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12 M_DATA_B[0..63] <<< M_DATA_B[0..63]

M_DATA_B0 AD34
M_DATA_B1 AD35
M_DATA_B2 AG35
M_DATA_B3 AH35
M_DATA_B4 AE35
M_DATA_B5 AE34
M_DATA_B6 AG34
M_DATA_B7 AH34
M_DATA_B8 AK35
M_DATA_B9 AL35
M_DATA_B10 AK32
M_DATA_B11 AL32
M_DATA_B12 AK34
M_DATA_B13 AL34
M_DATA_B14 AK31
M_DATA_B15 AL31
M_DATA_B16 AP35
M_DATA_B17 AN35
M_DATA_B18 AN32
M_DATA_B19 AP32
M_DATA_B20 AN34
M_DATA_B21 AP34
M_DATA_B22 AN31
M_DATA_B23 AP31
M_DATA_B24 AL29
M_DATA_B25 AM29
M_DATA_B26 AP29
M_DATA_B27 AR29
M_DATA_B28 AM28
M_DATA_B29 AL28
M_DATA_B30 AR28
M_DATA_B31 AP28
M_DATA_B32 AR12
M_DATA_B33 AP12
M_DATA_B34 AM13
M_DATA_B35 AL13
M_DATA_B36 AR13
M_DATA_B37 AP13
M_DATA_B38 AM12
M_DATA_B39 AL12
M_DATA_B40 AP10
M_DATA_B41 AR10
M_DATA_B42 AR7
M_DATA_B43 AP7
M_DATA_B44 AR9
M_DATA_B45 AP9
M_DATA_B46 AR6
M_DATA_B47 AP6
M_DATA_B48 AM10
M_DATA_B49 AL10
M_DATA_B50 AM7
M_DATA_B51 AL7
M_DATA_B52 AM9
M_DATA_B53 AL9
M_DATA_B54 AM6
M_DATA_B55 AL6
M_DATA_B56 AJ6
M_DATA_B57 AJ7
M_DATA_B58 AE6
M_DATA_B59 AE7
M_DATA_B60 AH7
M_DATA_B61 AH6
M_DATA_B62 AE7
M_DATA_B63 AE6

AR25
AR26
AM26
AM25
AP26
AP25
AL25
AL26
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]

CPU1B

BIOSTAR-D
SKYLAKE-S
Rev.0.7

DDR CHANNEL B

DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]

DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[5]/DDR1_BA[1]
DDR1_BA[2]/DDR1_CAB[5]/DDR1_BG[0]

DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]

DDR1_MA[3]/DDR1_CAB[4]/DDR1_MA[3]
DDR1_MA[4]/DDR1_CAB[3]/DDR1_MA[4]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]

DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]

DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]

DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#

DDR1_PAR
DDR1_ALERT#

DDR1_QOSN[0]/DDR0_QOSN[2]
DDR1_QOSN[1]/DDR0_QOSN[3]
DDR1_QOSN[2]/DDR0_QOSN[6]
DDR1_QOSN[3]/DDR0_QOSN[7]
DDR1_QOSN[4]/DDR1_QOSN[2]
DDR1_QOSN[5]/DDR1_QOSN[3]
DDR1_QOSN[6]
DDR1_QOSN[7]

DDR1_QOSP[0]/DDR0_QOSP[2]
DDR1_QOSP[1]/DDR0_QOSP[3]
DDR1_QOSP[2]/DDR0_QOSP[6]
DDR1_QOSP[3]/DDR0_QOSP[7]
DDR1_QOSP[4]/DDR1_QOSP[2]
DDR1_QOSP[5]/DDR1_QOSP[3]
DDR1_QOSP[6]
DDR1_QOSP[7]

DDR1_QOSP[8]
DDR1_QOSP[8]

DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ

2 OF 12

LGA 1151 SOCKET

AM20 >>> CK_M_CH1_0_DP 12
AM21 >>> CK_M_CH1_0_DN 12
AP22 >>> CK_M_CH1_1_DP 12
AP21 >>> CK_M_CH1_1_DN 12
AN20
AN21
AP19
AP20
DDR1_CK[3]

AY29 >>> M_SCKE_B0 12
AY29 >>> M_SCKE_B1 12
AW29
AU29

AP17 >>> M_SCS_B_N0 12
AN15 >>> M_SCS_B_N1 12
AN17
AM15

AL16 >>> M_ODT_B0 12
AL16 >>> M_ODT_B1 12
AP15
AL15

AN18 M_MAA_B16 >>> M_MAA_B[0..16] 12
AL17 M_MAA_B14 >>> M_MAA_B[0..16] 12
AP16 M_MAA_B15 >>> M_MAA_B[0..16] 12

AL18 >>> M_SBS_B0 12
AM18 >>> M_SBS_B1 12
AW28 >>> M_BG_CH1_0 12

AL19 M_MAA_B0 >>> M_MAA_B[0..16] 12
AL22 M_MAA_B1 >>> M_MAA_B[0..16] 12
AM22 M_MAA_B2 >>> M_MAA_B[0..16] 12
AM23 M_MAA_B3 >>> M_MAA_B[0..16] 12
AP23 M_MAA_B4 >>> M_MAA_B[0..16] 12
AW23 M_MAA_B5 >>> M_MAA_B[0..16] 12
AW23 M_MAA_B6 >>> M_MAA_B[0..16] 12
AY26 M_MAA_B7 >>> M_MAA_B[0..16] 12
AU26 M_MAA_B8 >>> M_MAA_B[0..16] 12
AW27 M_MAA_B9 >>> M_MAA_B[0..16] 12
AP18 M_MAA_B10 >>> M_MAA_B[0..16] 12
AU27 M_MAA_B11 >>> M_MAA_B[0..16] 12
AY27 M_MAA_B12 >>> M_MAA_B[0..16] 12
AR15 M_MAA_B13 >>> M_MAA_B[0..16] 12

AY28 >>> M_BG_CH1_1 12
AU28 >>> DDR_CH1_ACT_N 12

AL20 >>> DDR_CH1_PAR 12
AY25 >>> DDR_CH1_ALERT_N 12

AF34 >>> M_DQS_B_DN0 12
AK33 >>> M_DQS_B_DN1 12
AN33 >>> M_DQS_B_DN2 12
AN29 >>> M_DQS_B_DN3 12
AN13 >>> M_DQS_B_DN4 12
AR8 >>> M_DQS_B_DN5 12
AM8 >>> M_DQS_B_DN6 12
AG6 >>> M_DQS_B_DN7 12

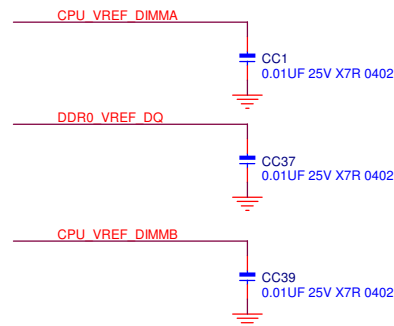
AF35 >>> M_DQS_B_DP0 12
AL33 >>> M_DQS_B_DP1 12
AP33 >>> M_DQS_B_DP2 12
AN28 >>> M_DQS_B_DP3 12
AN12 >>> M_DQS_B_DP4 12
AP8 >>> M_DQS_B_DP5 12
AL8 >>> M_DQS_B_DP6 12
AG7 >>> M_DQS_B_DP7 12

AN25
AN26

M_DQS_B_DP[0..7] <<< M_DQS_B_DP[0..7] 12

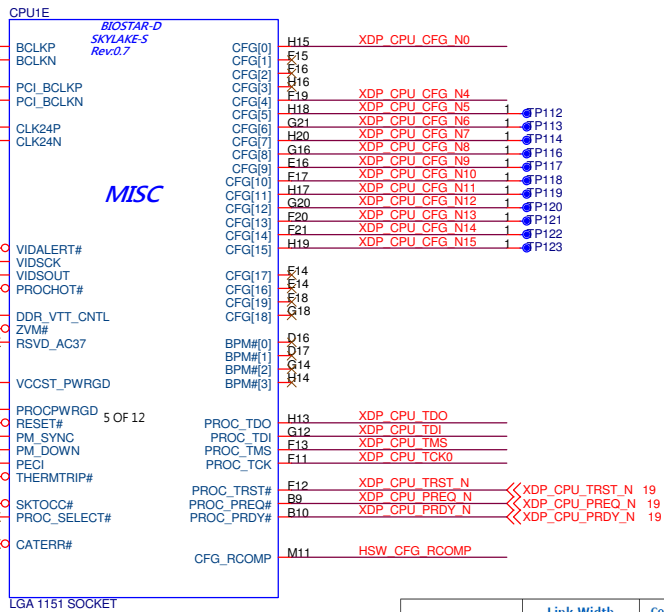
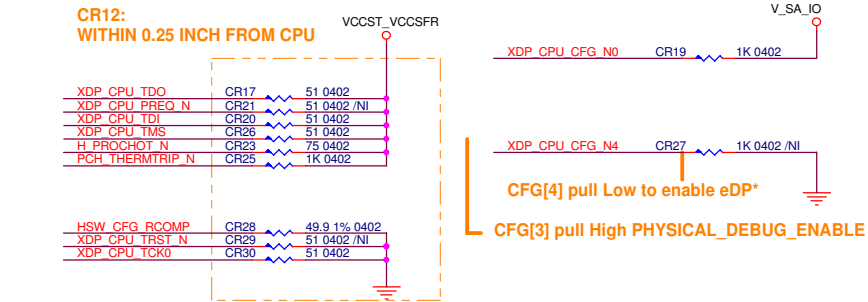
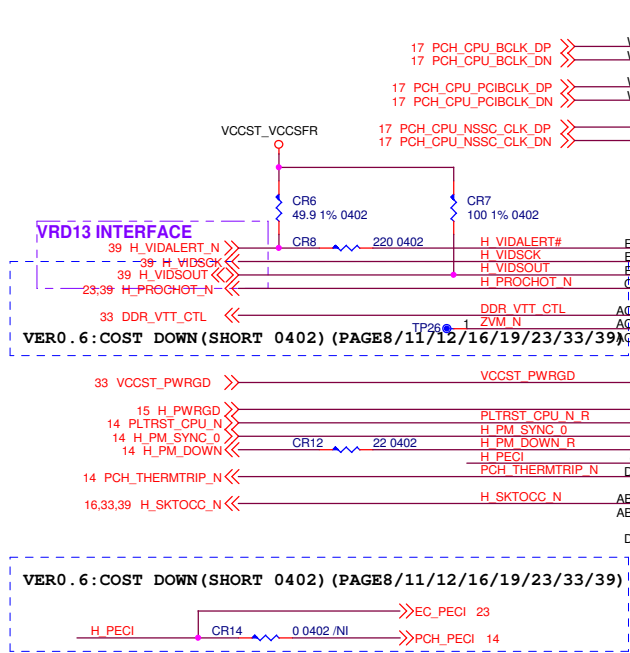
M_DQS_B_DN[0..7] <<< M_DQS_B_DN[0..7] 12

VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)



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Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 Reversed	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 Reversed	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 Reversed	x8	x4	x4	0	0	0

CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1'. If not terminated on the board, refer to the appropriate platform design guide for pull-downs.</p> <p>CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted.</p> <ul style="list-style-type: none">1 = (Configured) Normal Operation;0 = stall. <p>CFG[1]: Reserved configuration lane.</p> <p>CFG[2]: PCI Express* Static x16 Lane Reversal.</p> <ul style="list-style-type: none">1 = Normal operation.0 = Lane numbers reversed. <p>CFG[3]: Reserved configuration lane.</p> <p>CFG[4]: eDP enable.</p> <ul style="list-style-type: none">1 = Disabled.0 = Enabled. <p>CFG[5]: PCI Express* Bifurcation</p> <ul style="list-style-type: none">00 = 1 x16, 2 x8 PCI Express*01 = reserved10 = 2 x8 PCI Express*11 = 1 x16 PCI Express* <p>CFG[7]: PEG Training.</p> <ul style="list-style-type: none">1 = (Default) PEG Training immediately following RESET# de-assertion.0 = PEG Wait for BIOS for training. <p>CFG[10:15]: Reserved configuration lanes.</p>
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CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG_UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYN	PMSYNC ASYN MODE
14	RESERVED		
15	RESERVED		

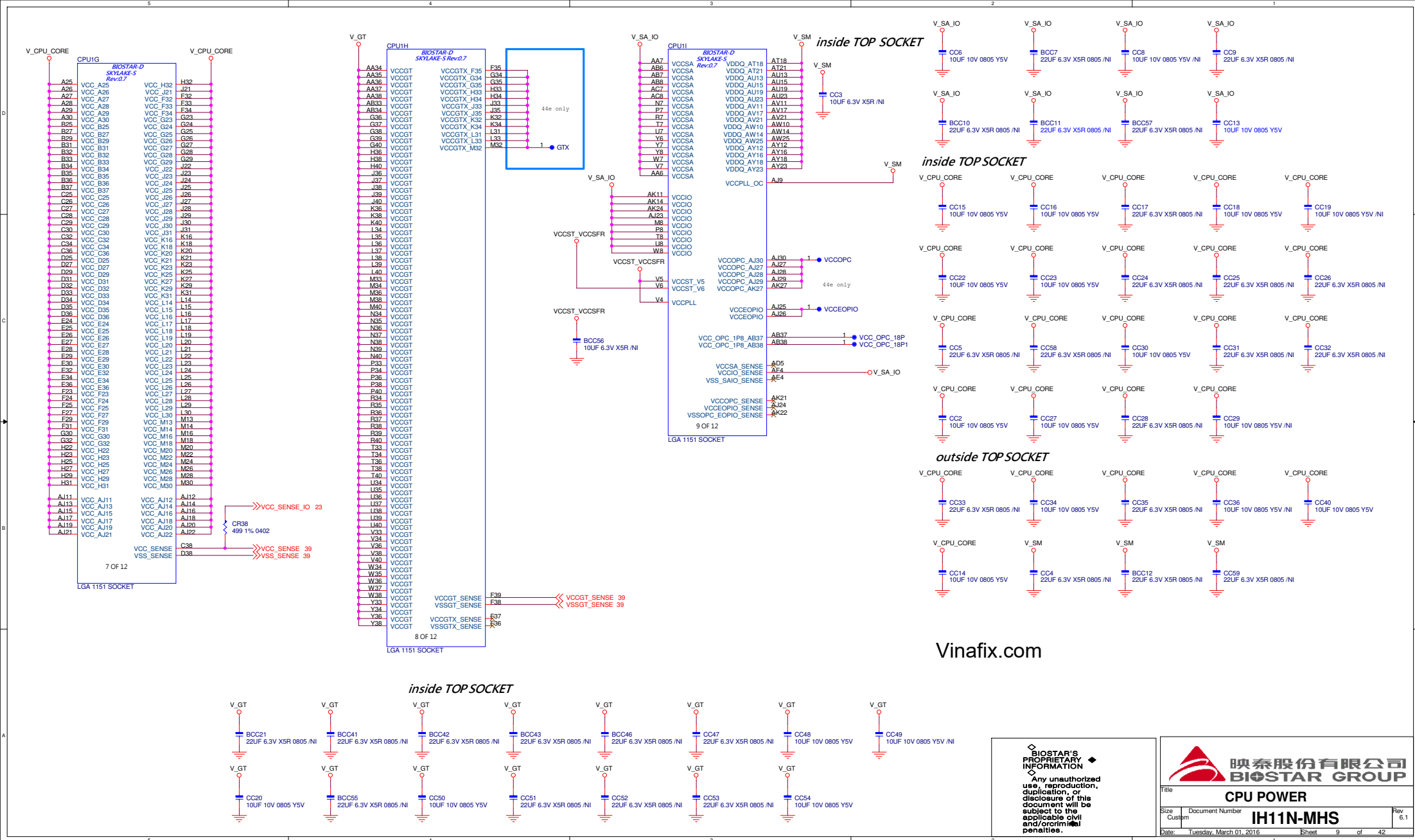
ALL PINS HAVE INTERNAL PULL-UPS

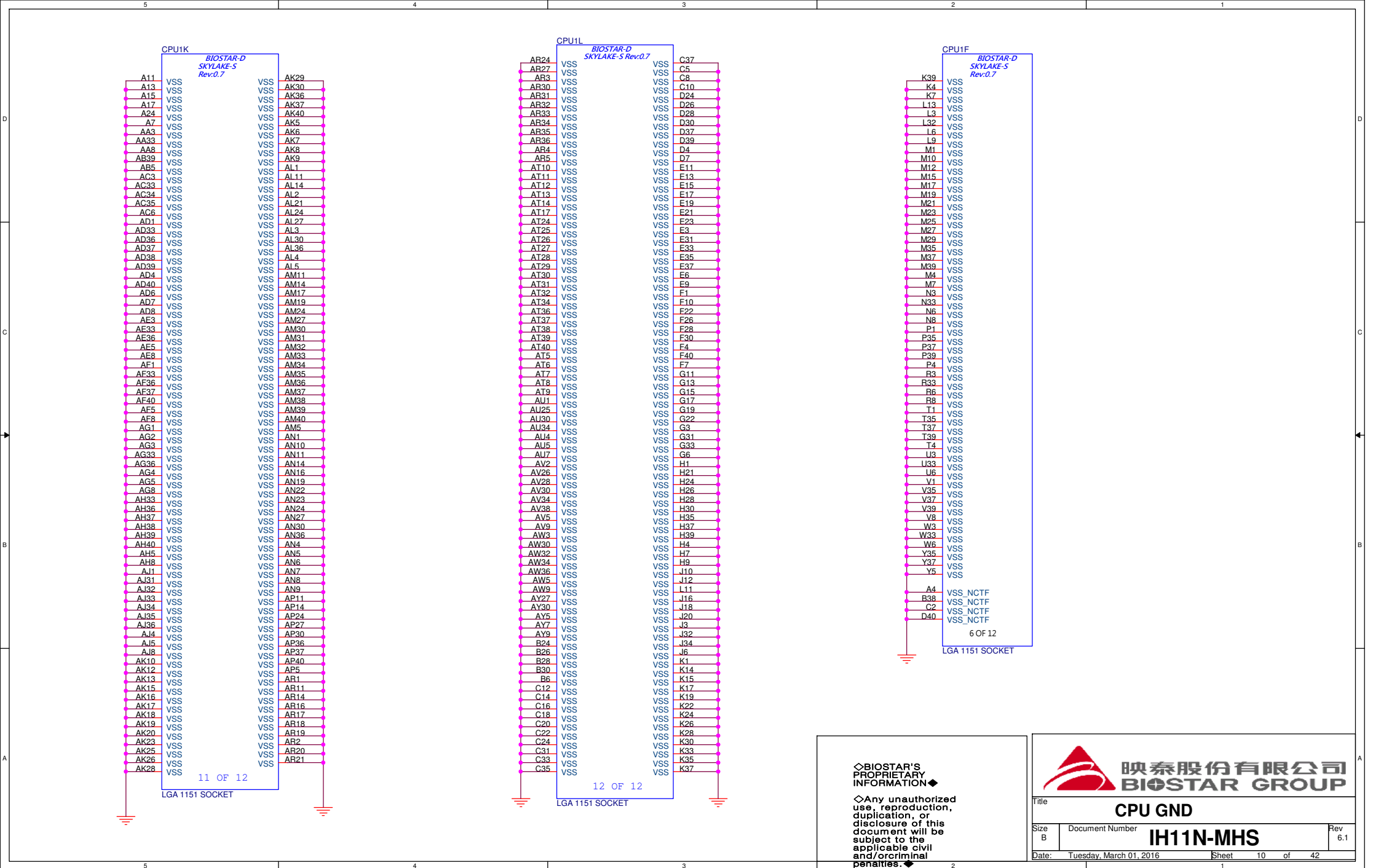
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CPU MISC

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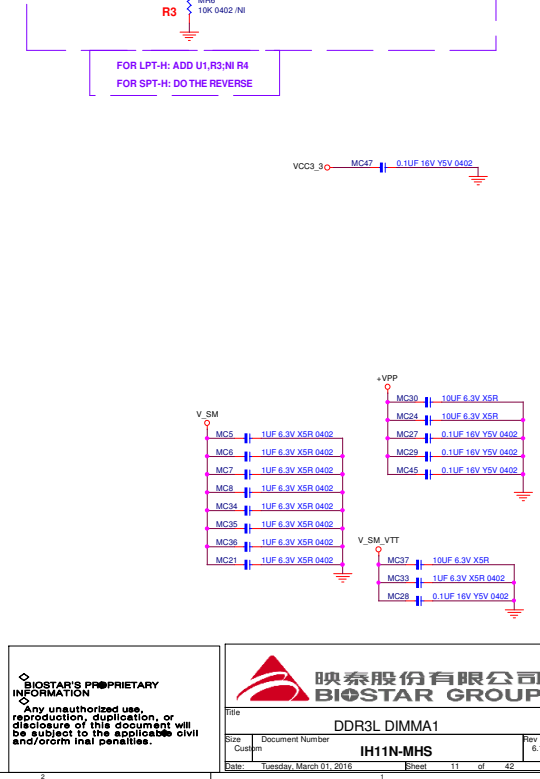
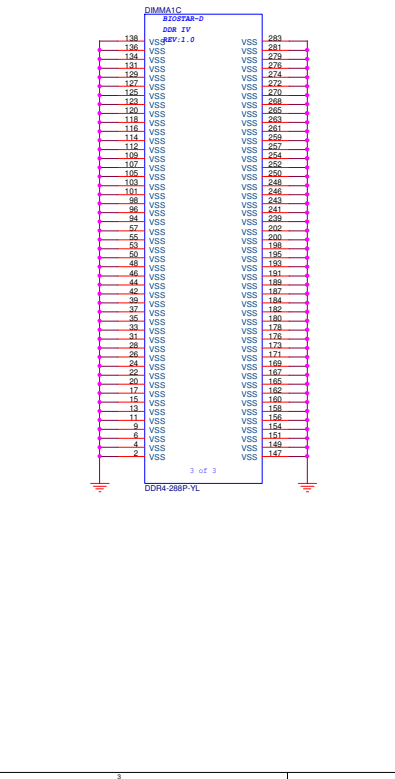
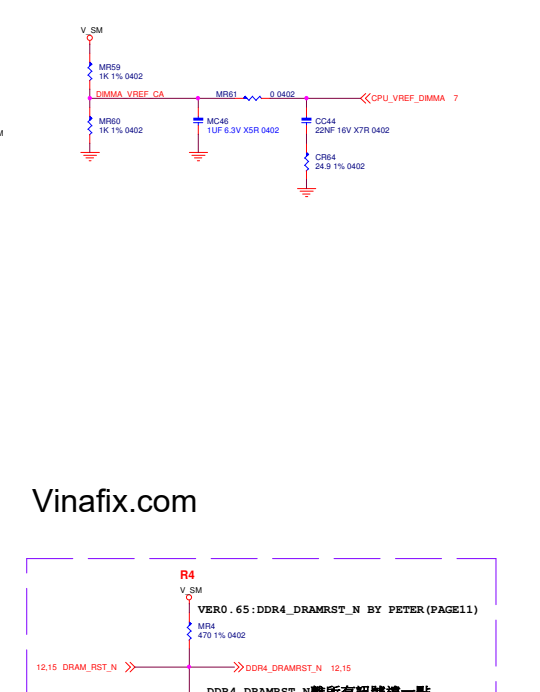
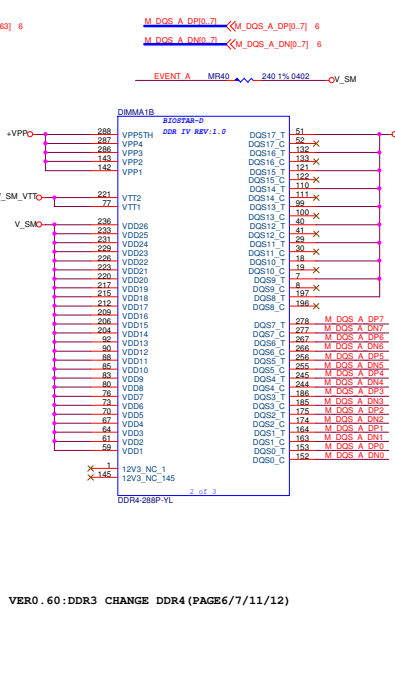
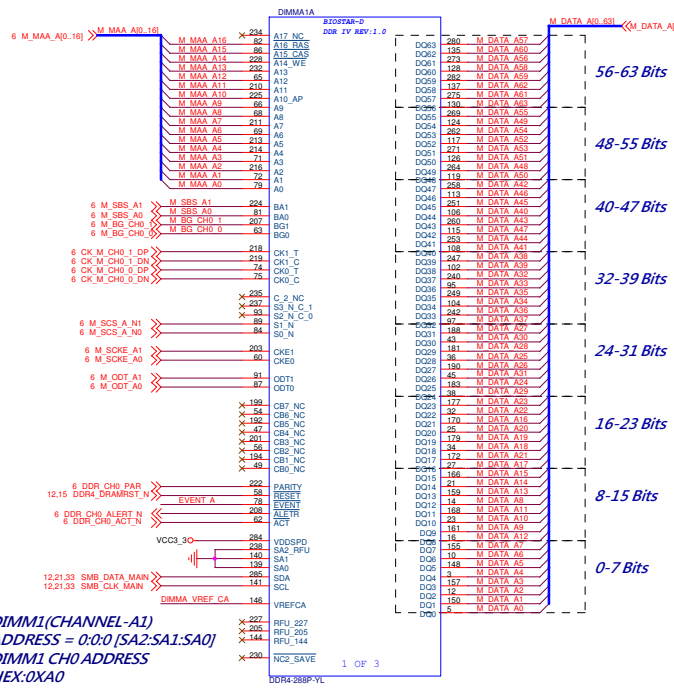


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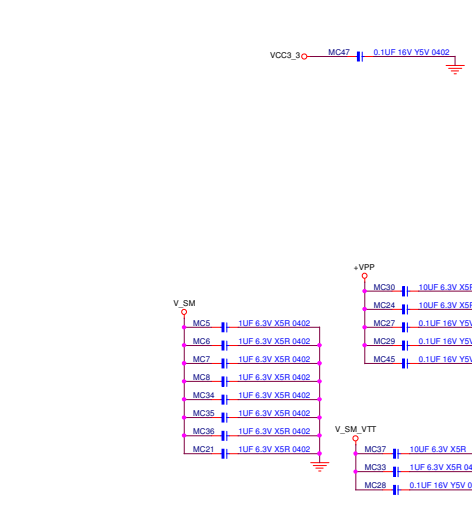
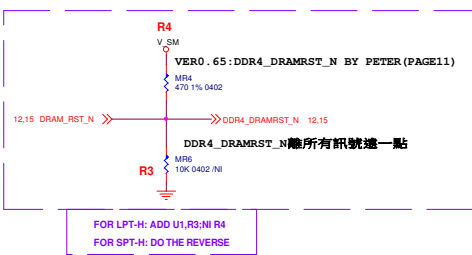
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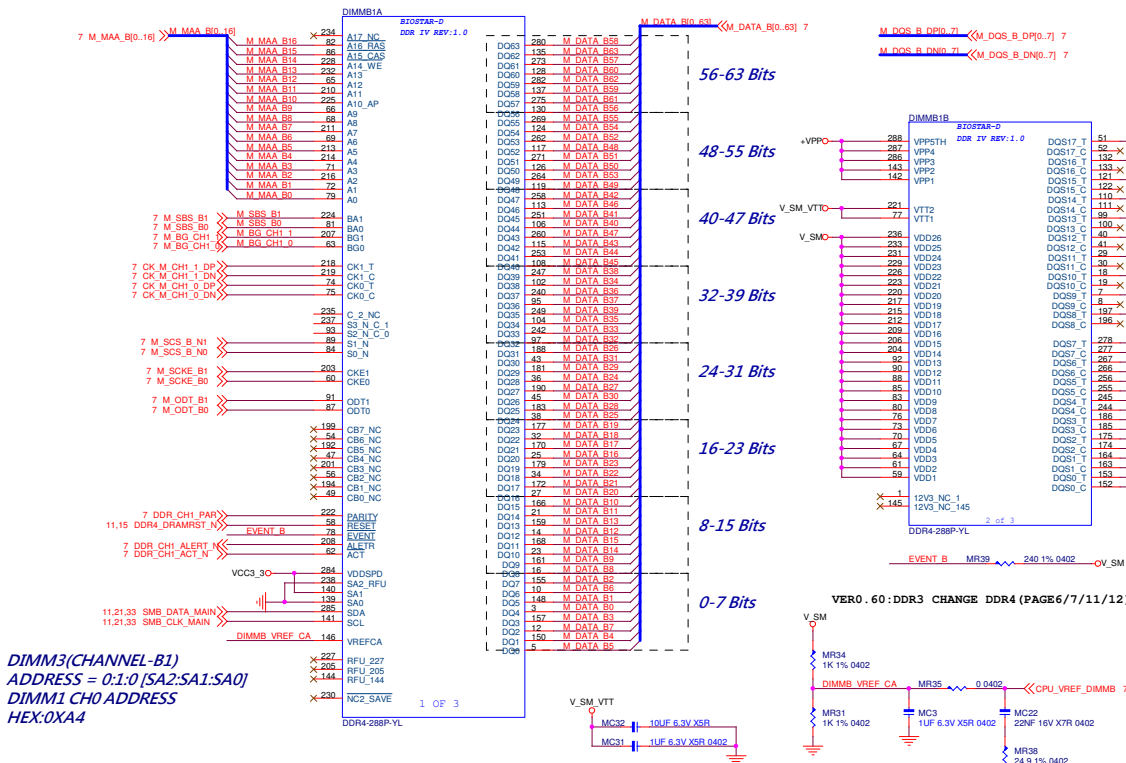


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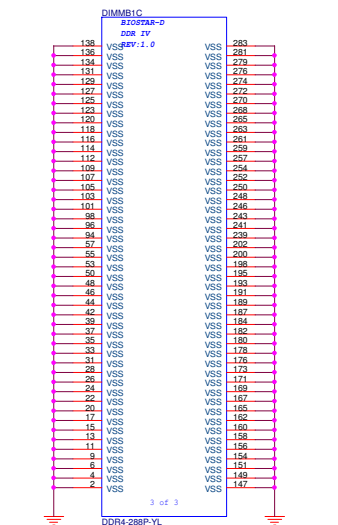
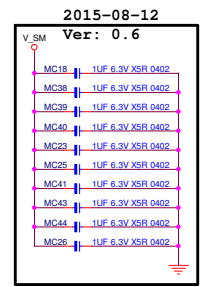
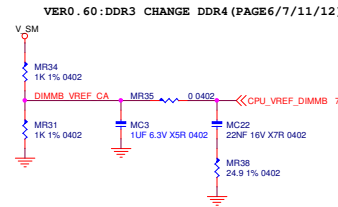


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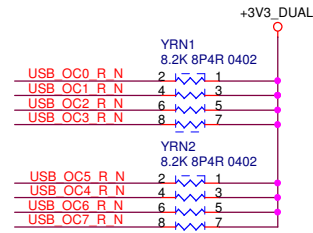
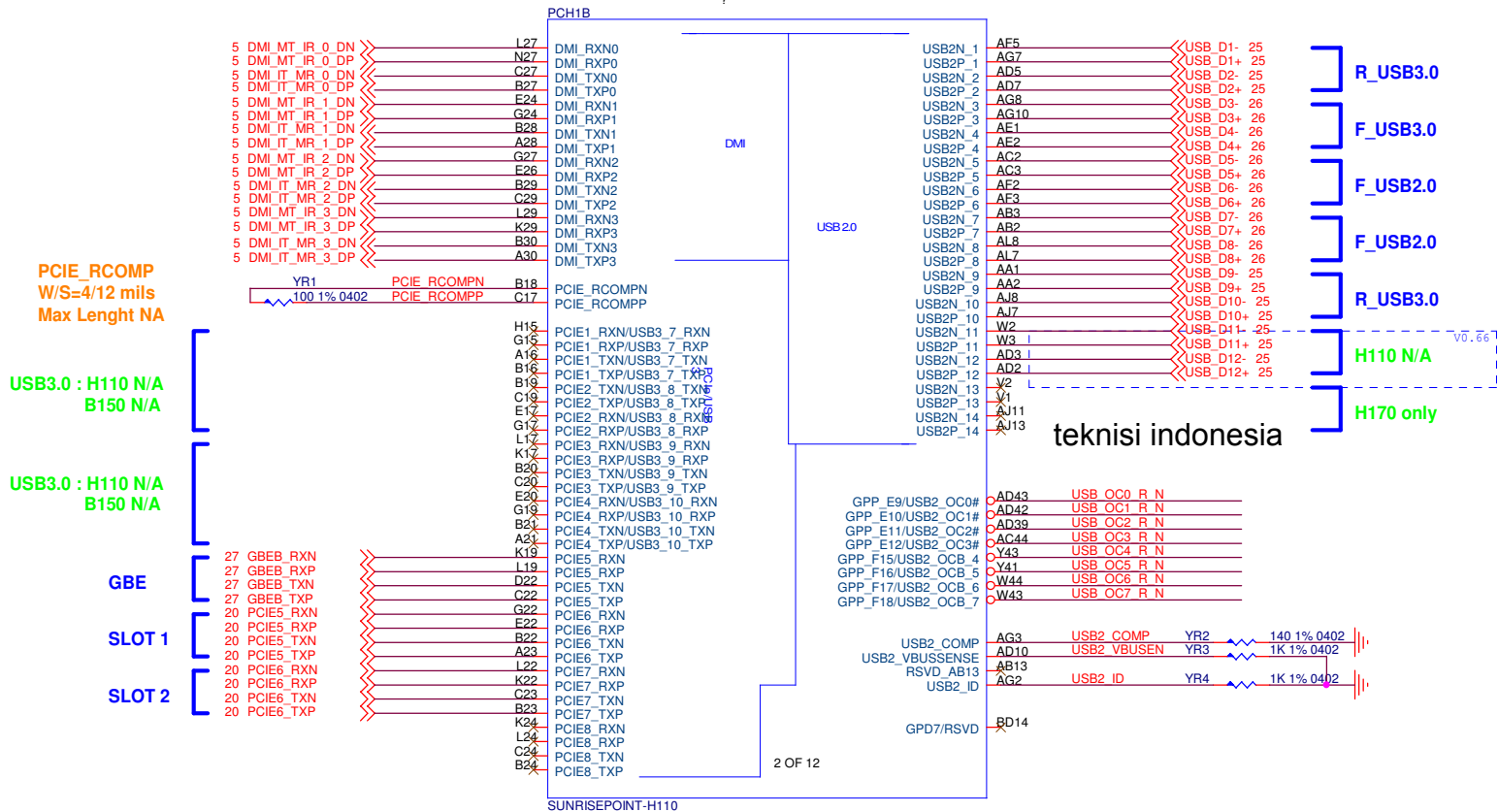




DIMM3(CHANNEL-B1)
DIMM3 ADDRESS = 0:1:0 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS
HEX:0XA4



PCH PART: Y+Reference

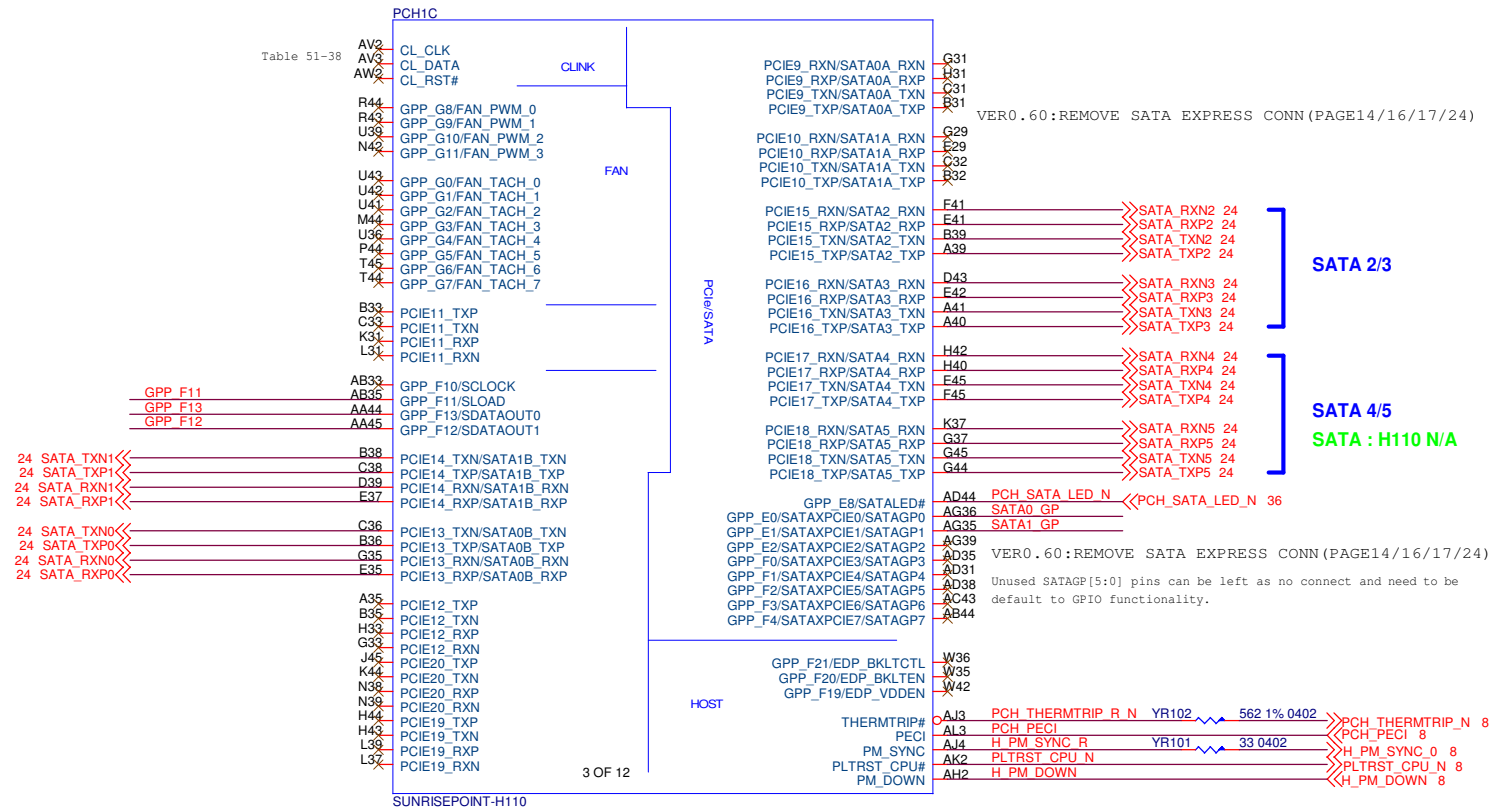
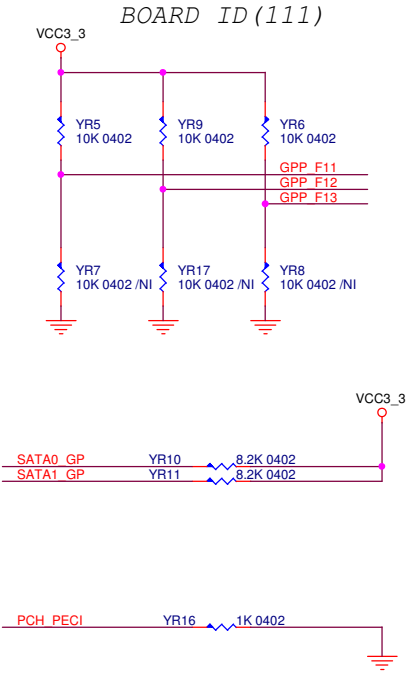


26	PCIe #20																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
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PCH PART: Y+Reference



GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

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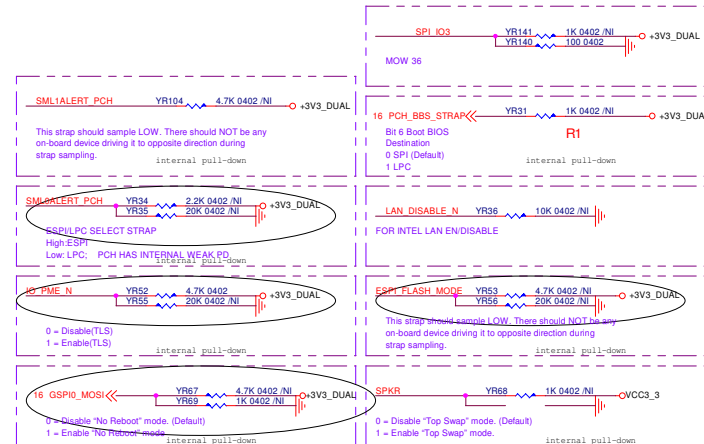
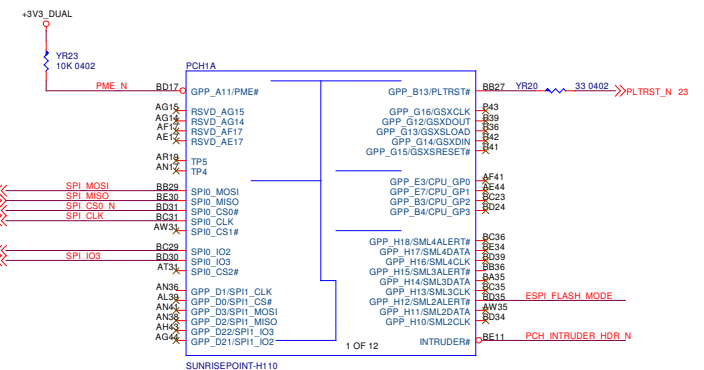
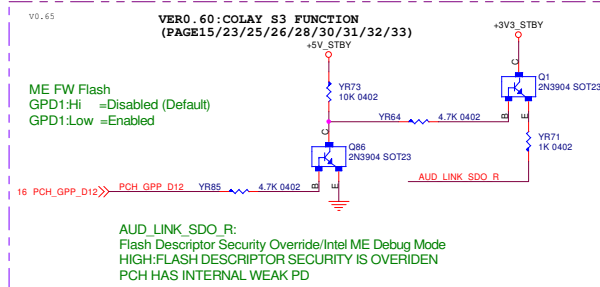
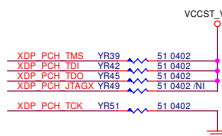
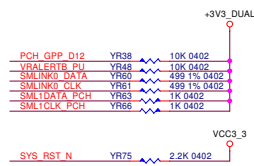
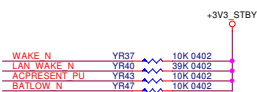
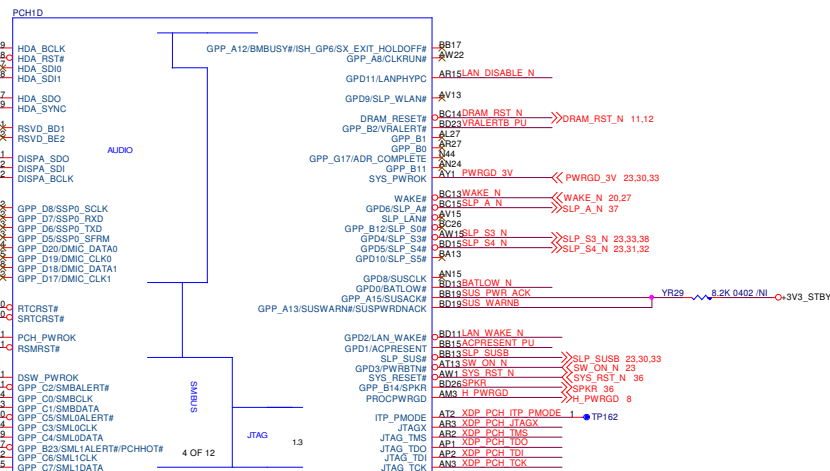
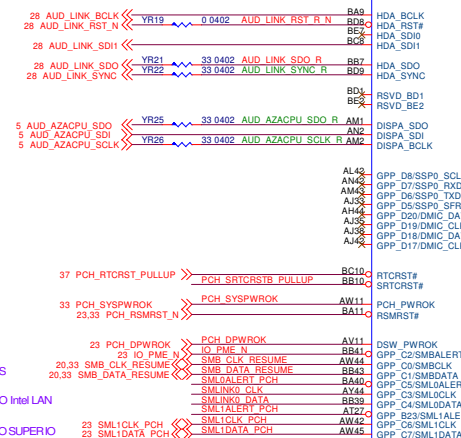
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Title PCH CLINK/SATA/CPU HOST

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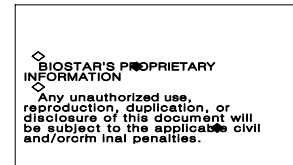


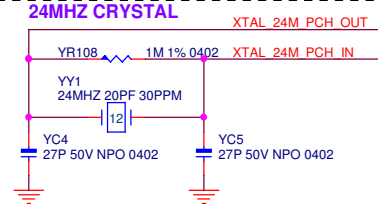
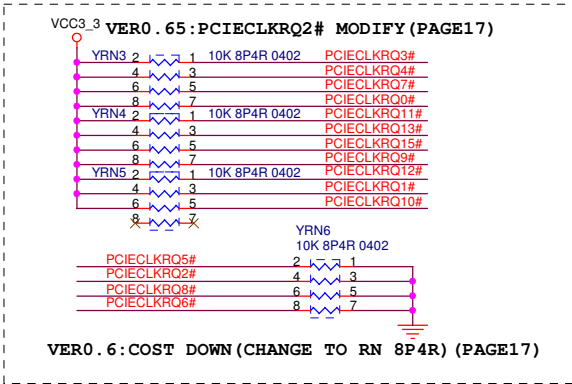
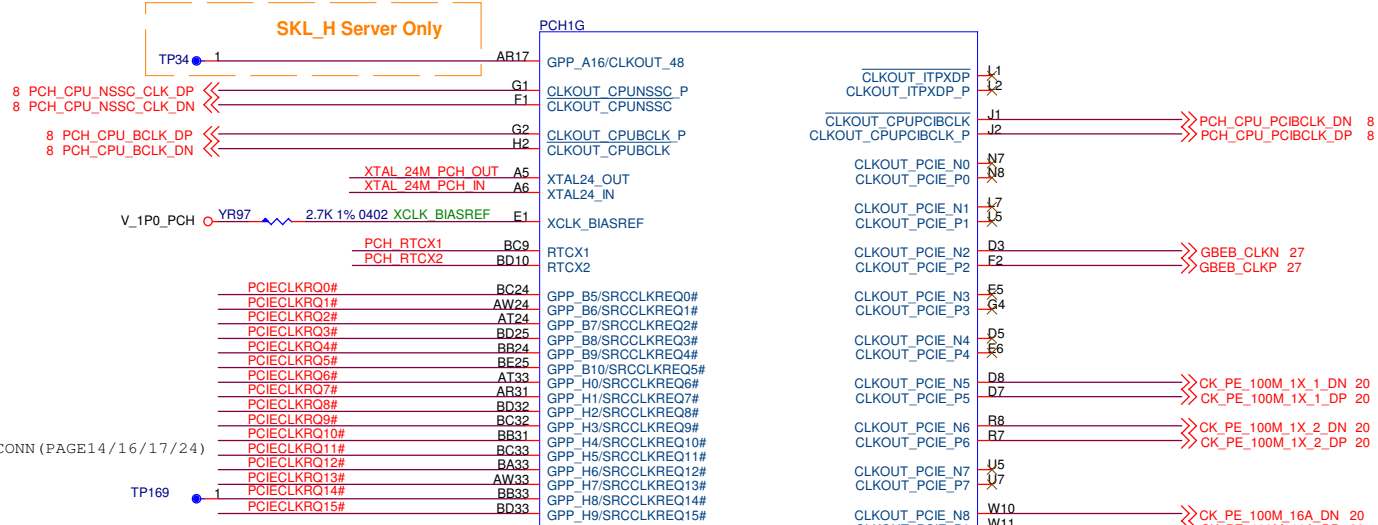
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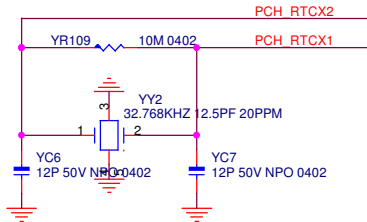
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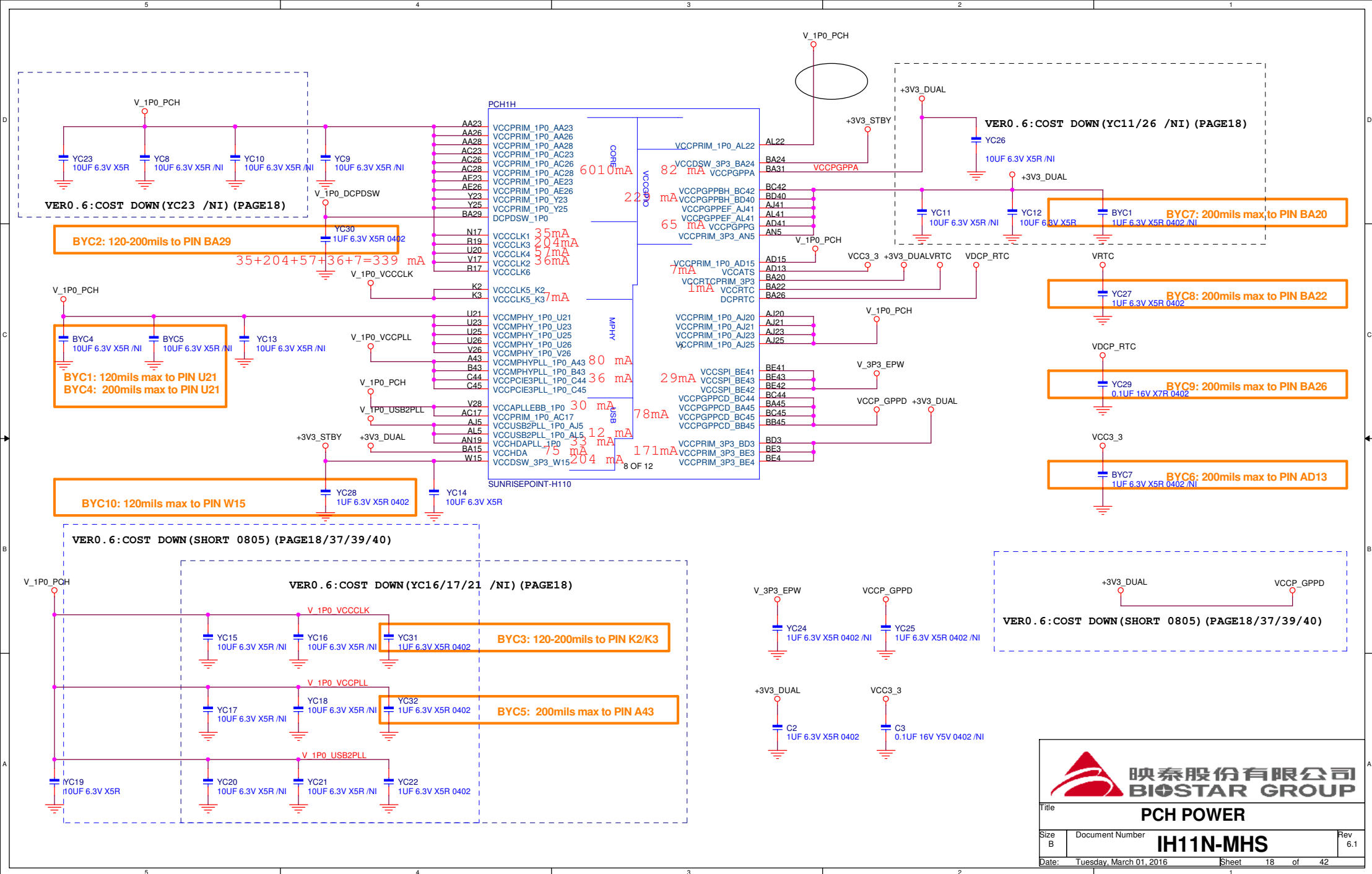
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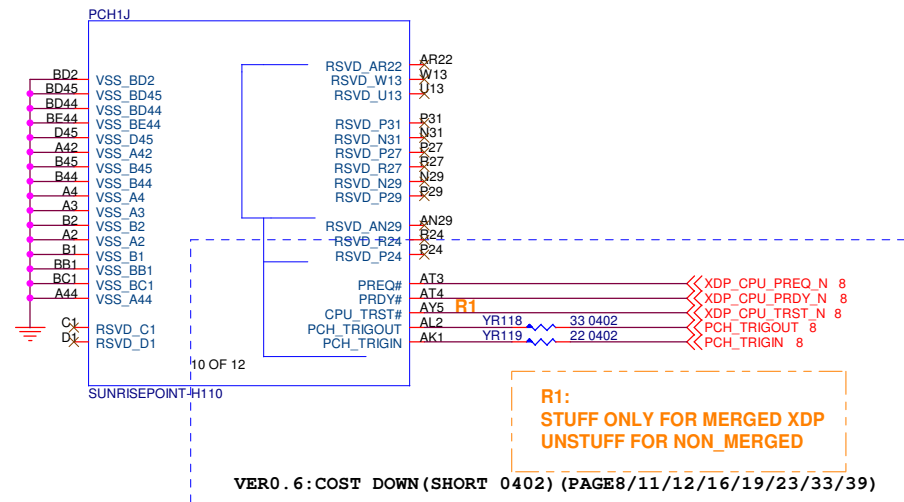
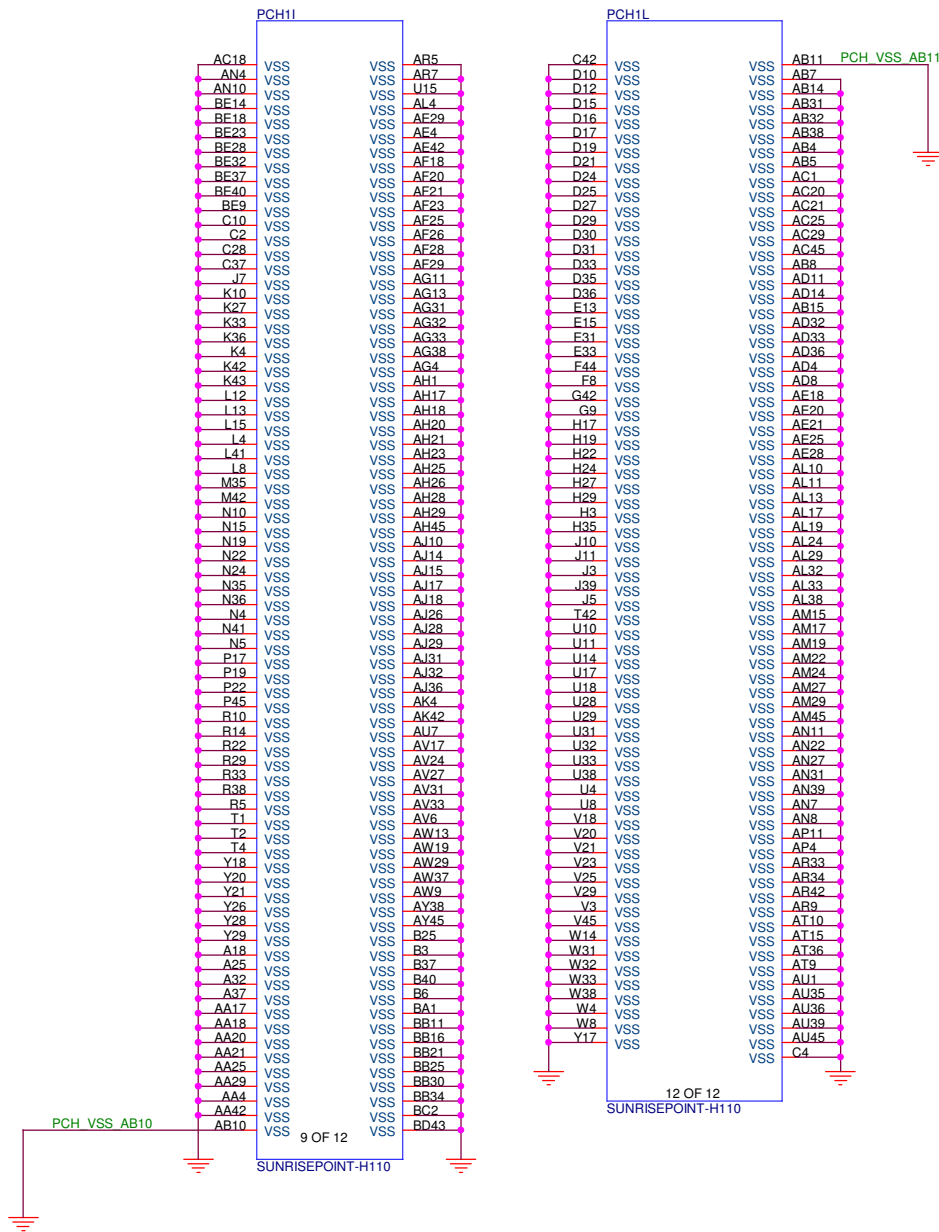
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PCIE X1


PCIE X16

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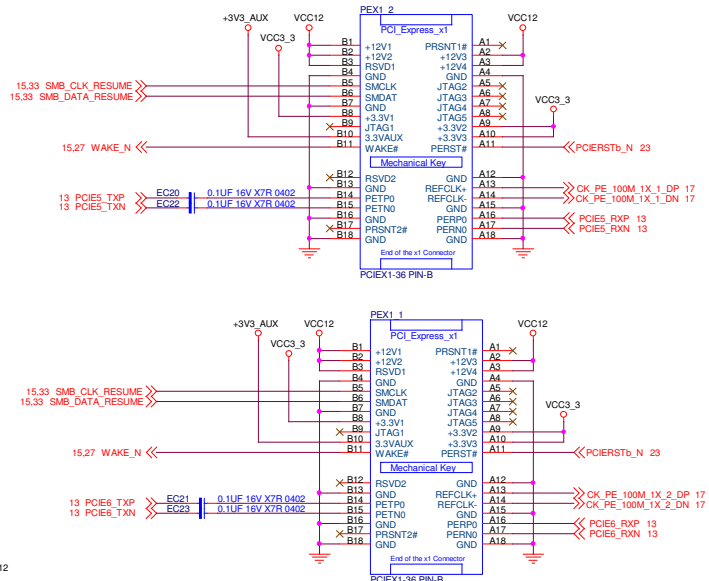
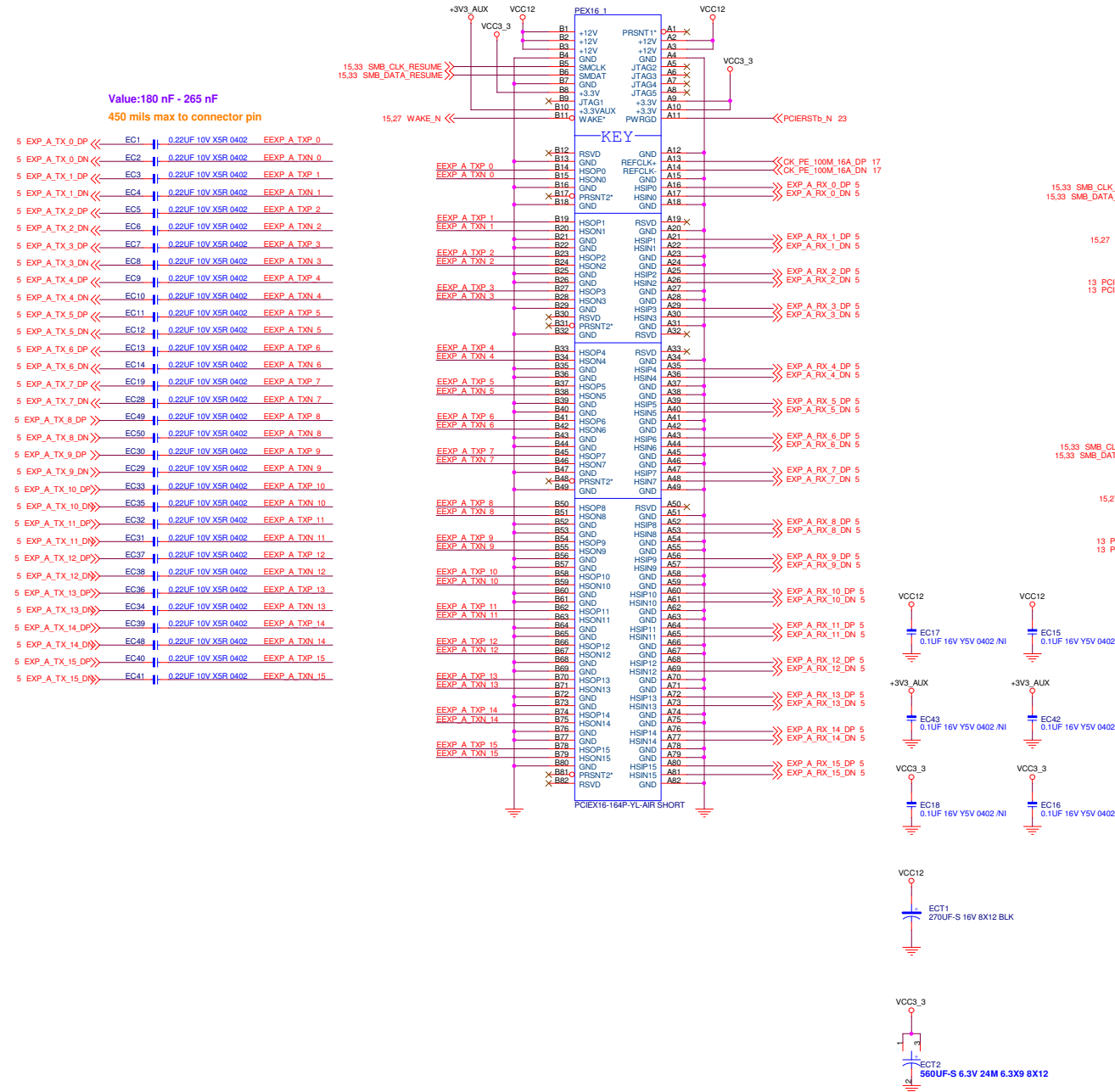




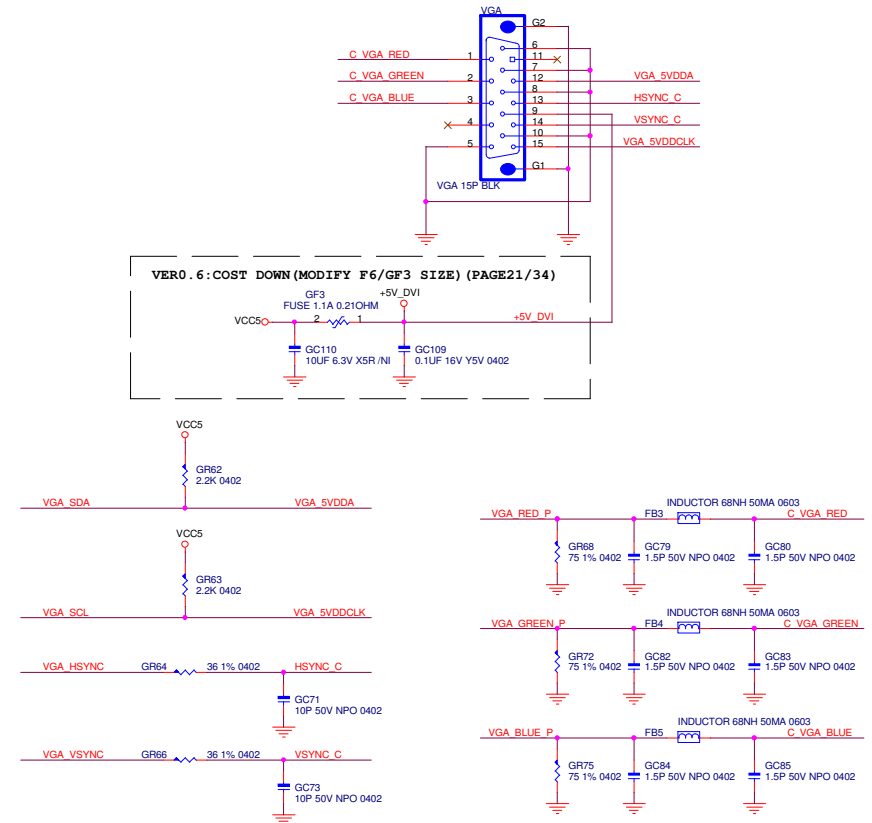
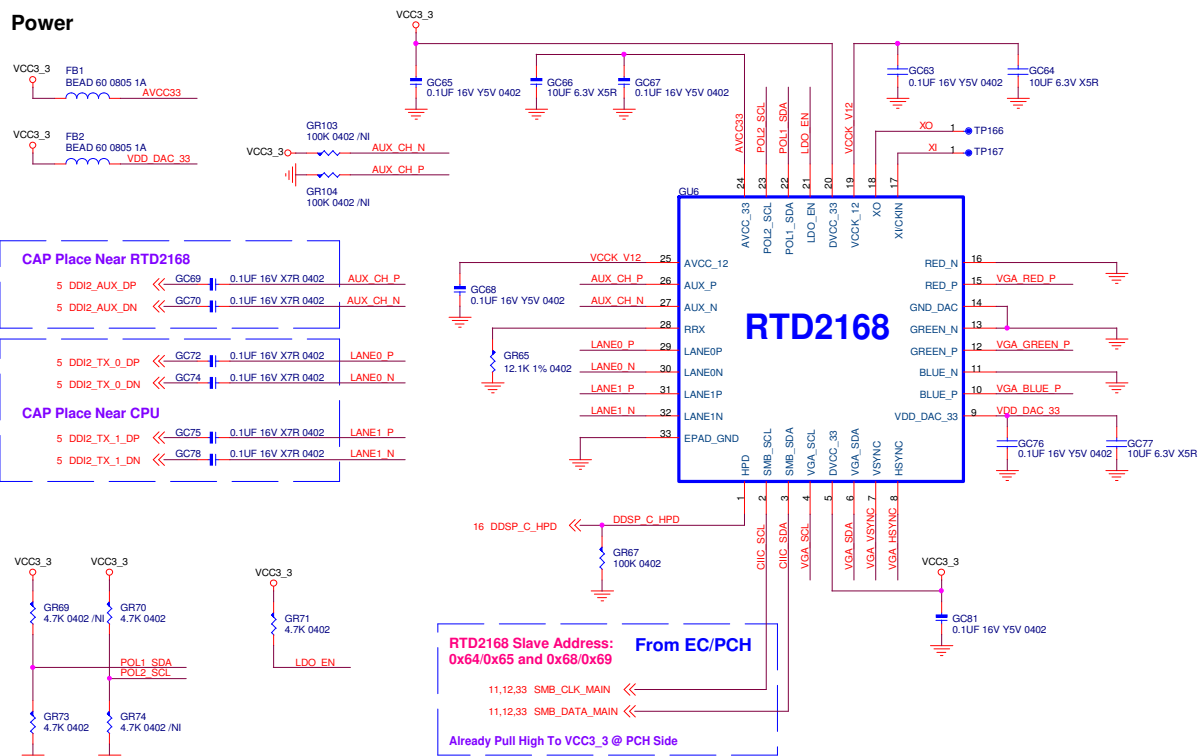
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SLOT PART: E+Reference



Power



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EPPROM MODE

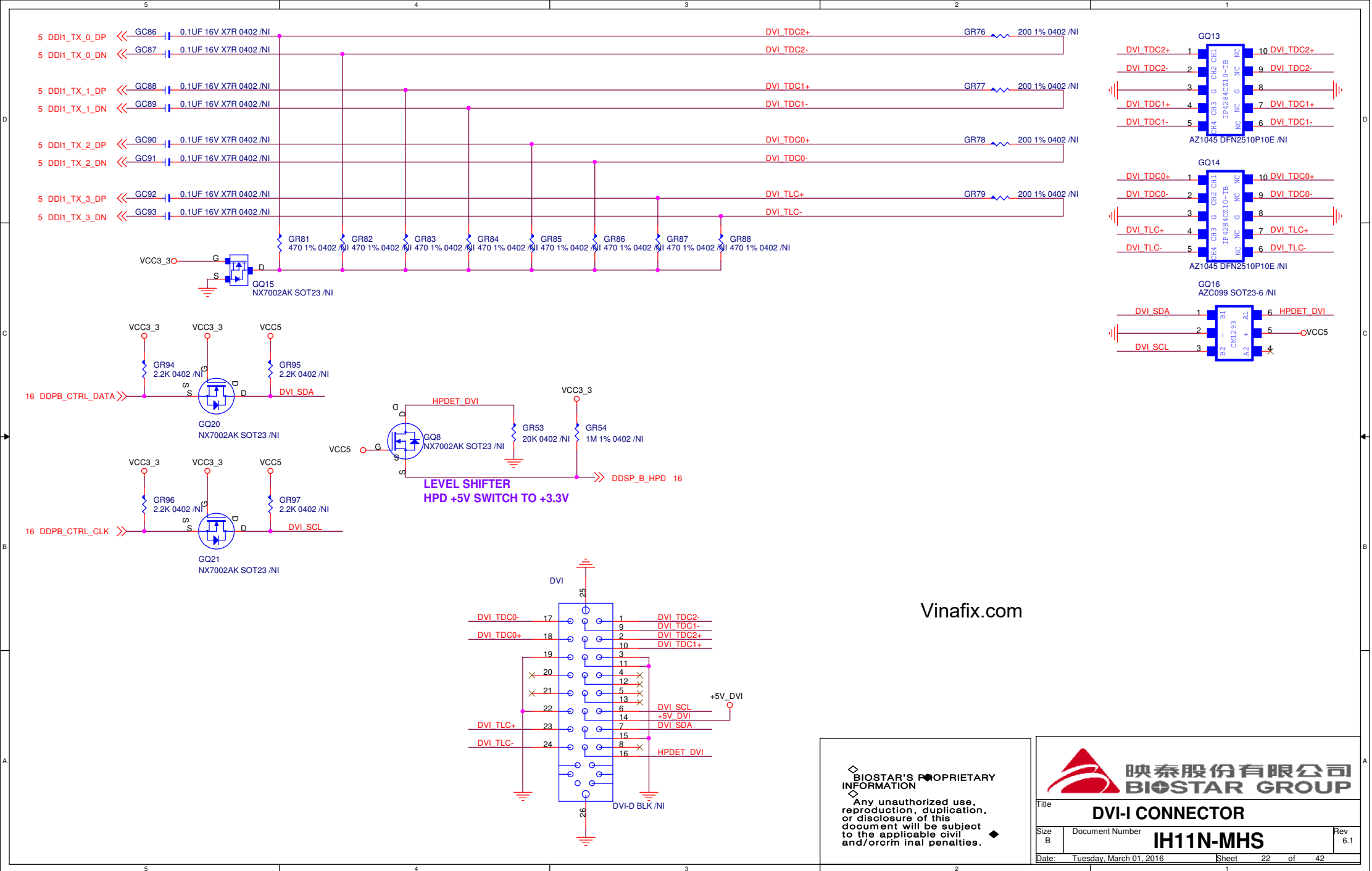
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Type	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW



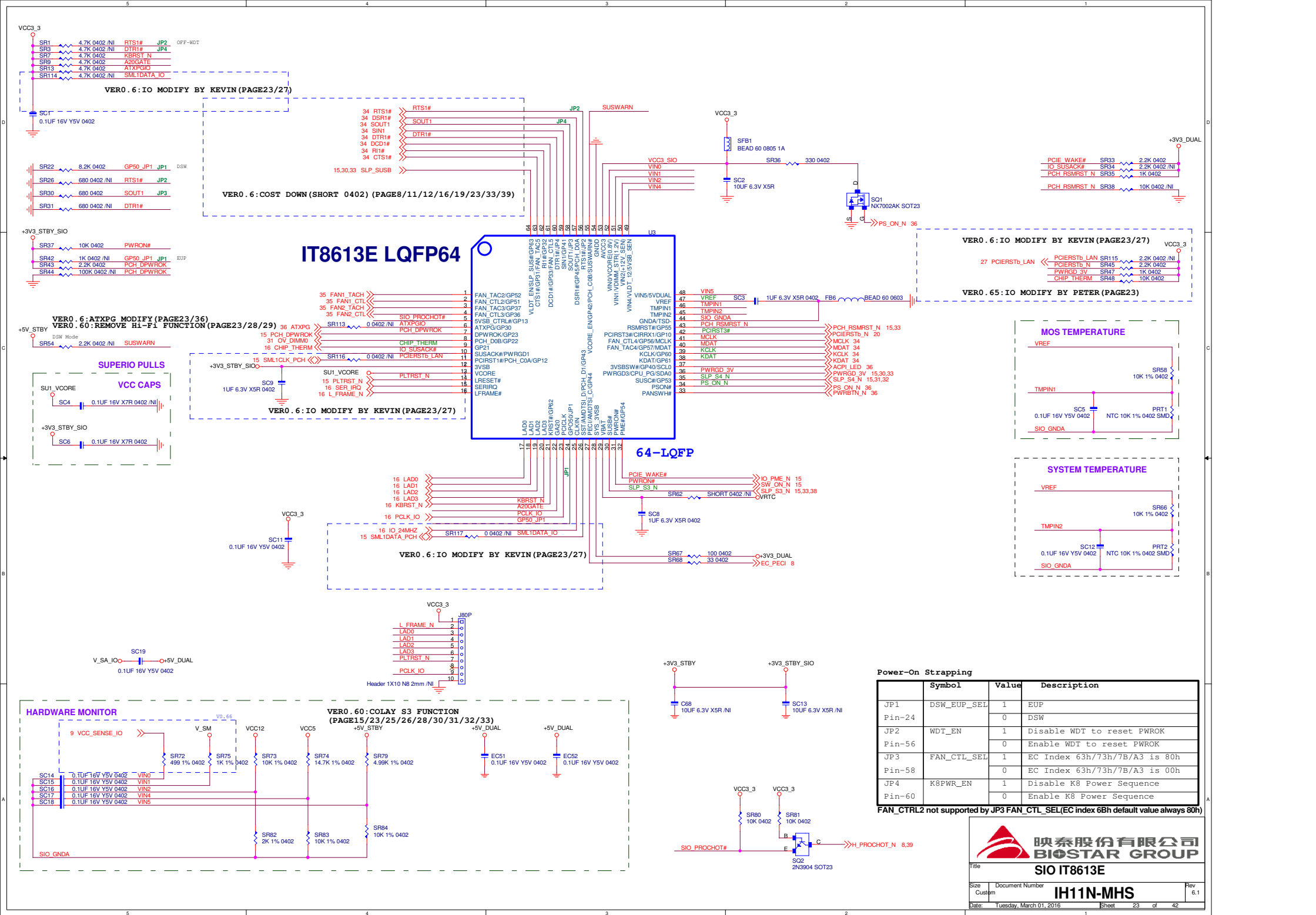


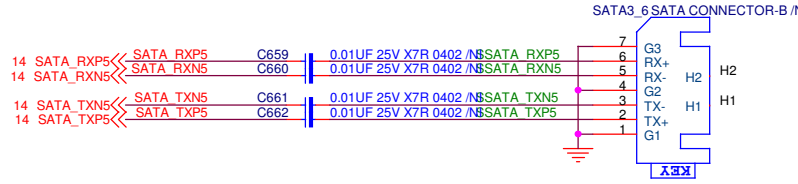
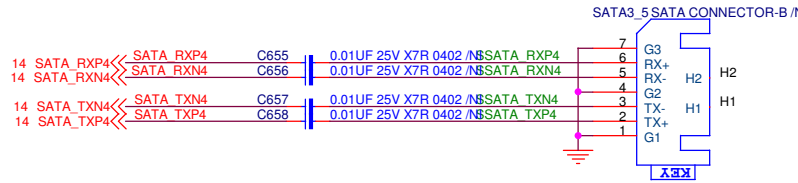
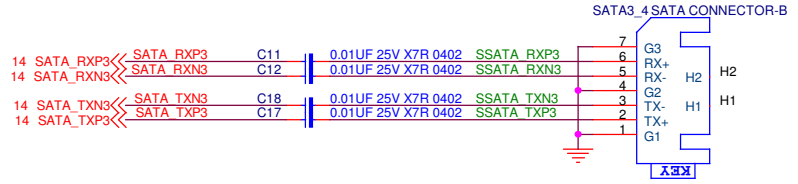
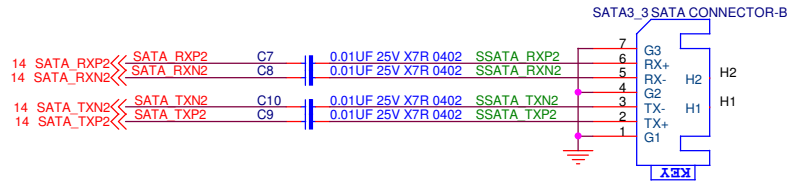
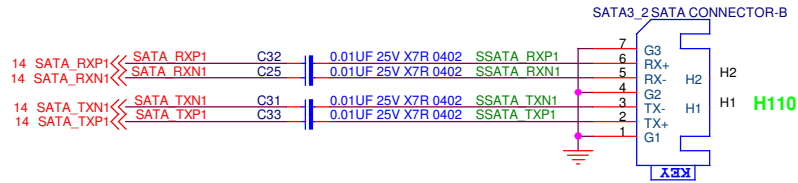
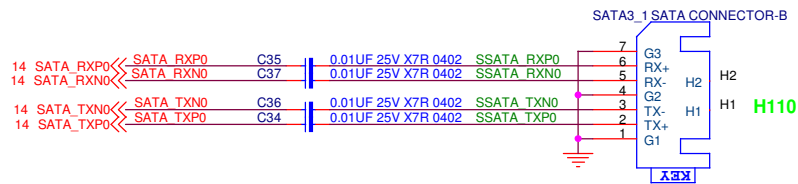
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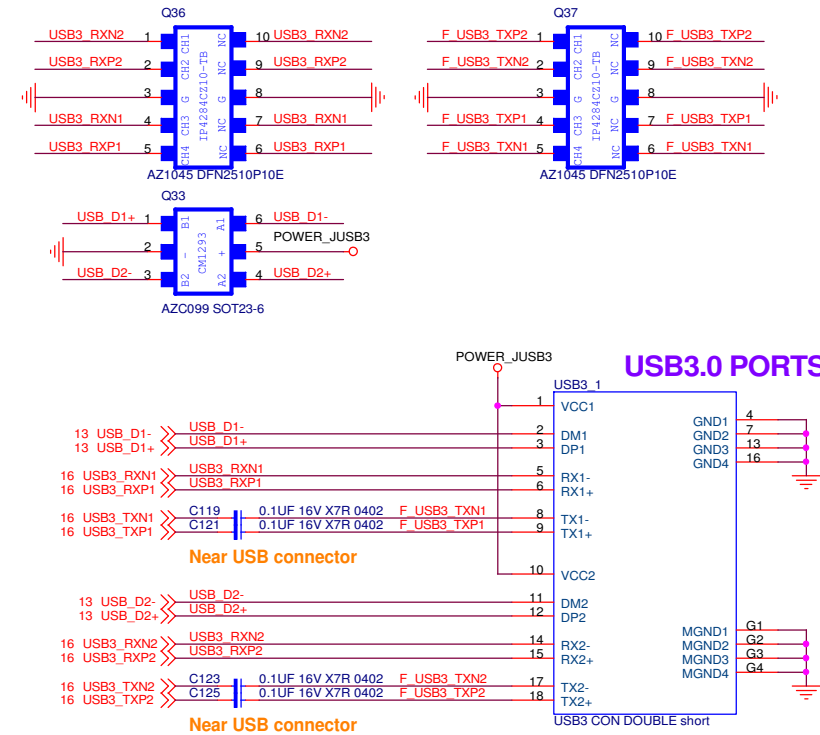
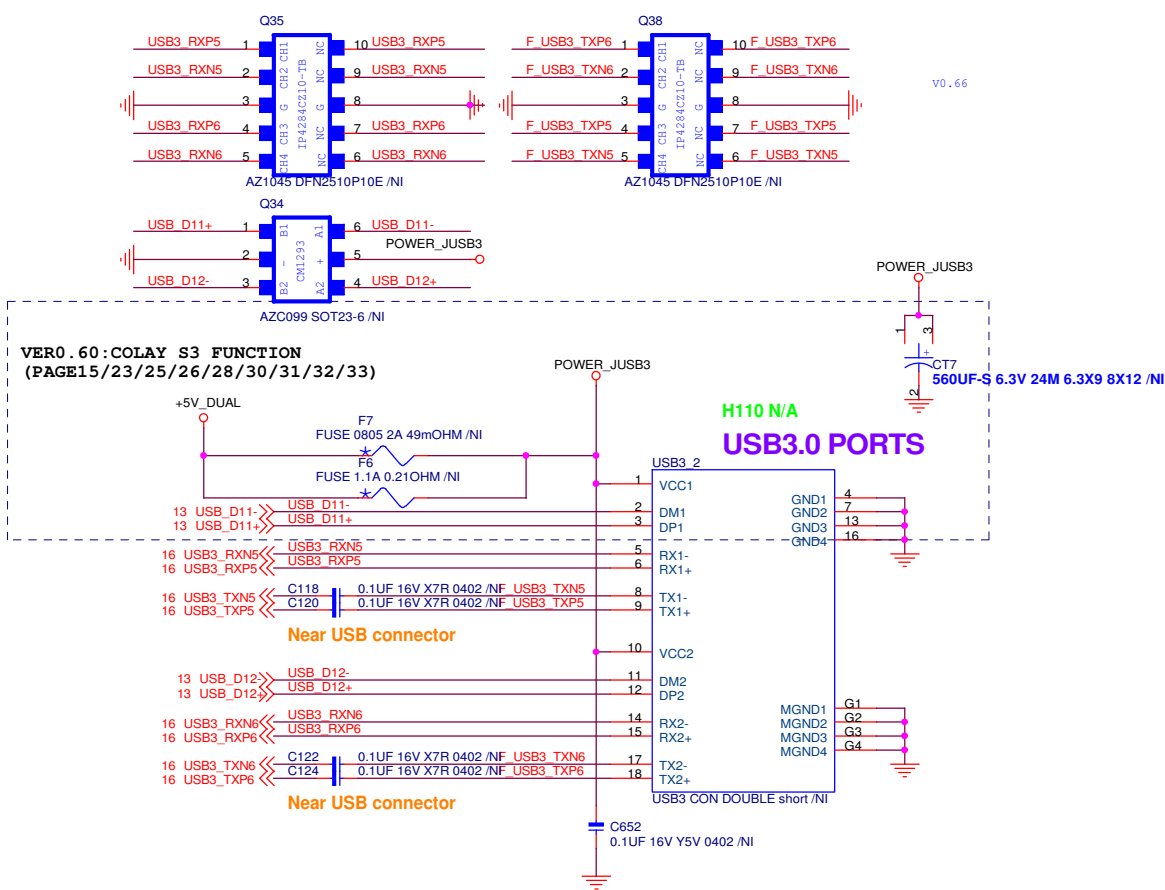
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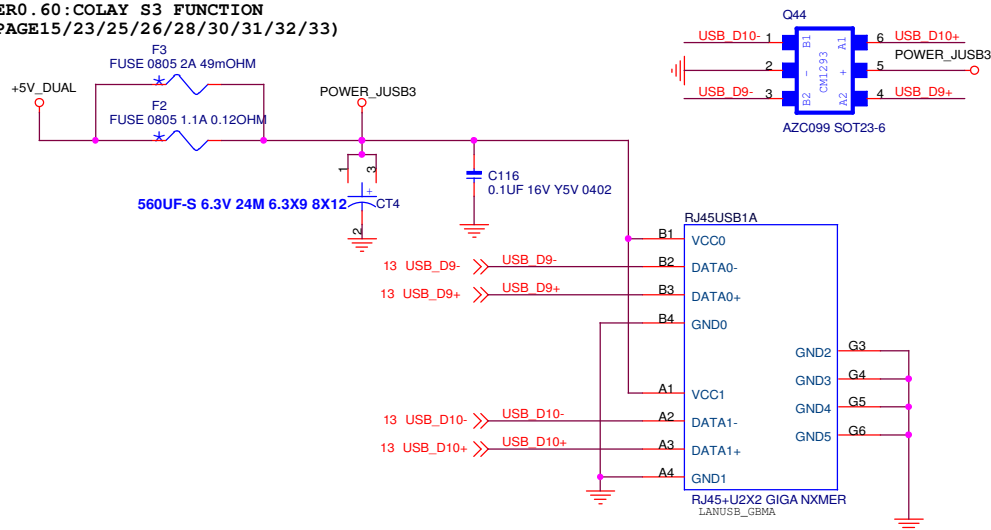


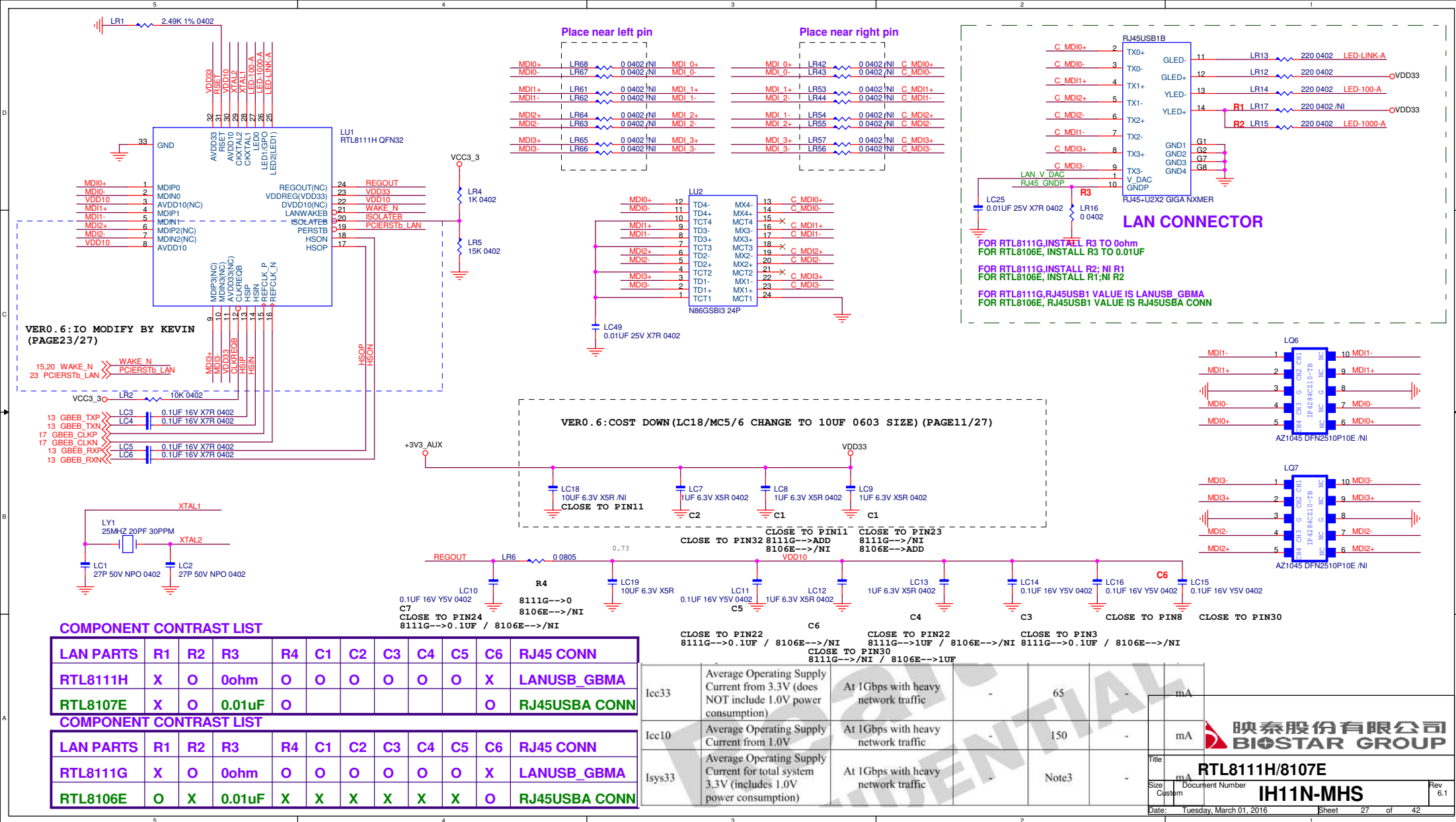
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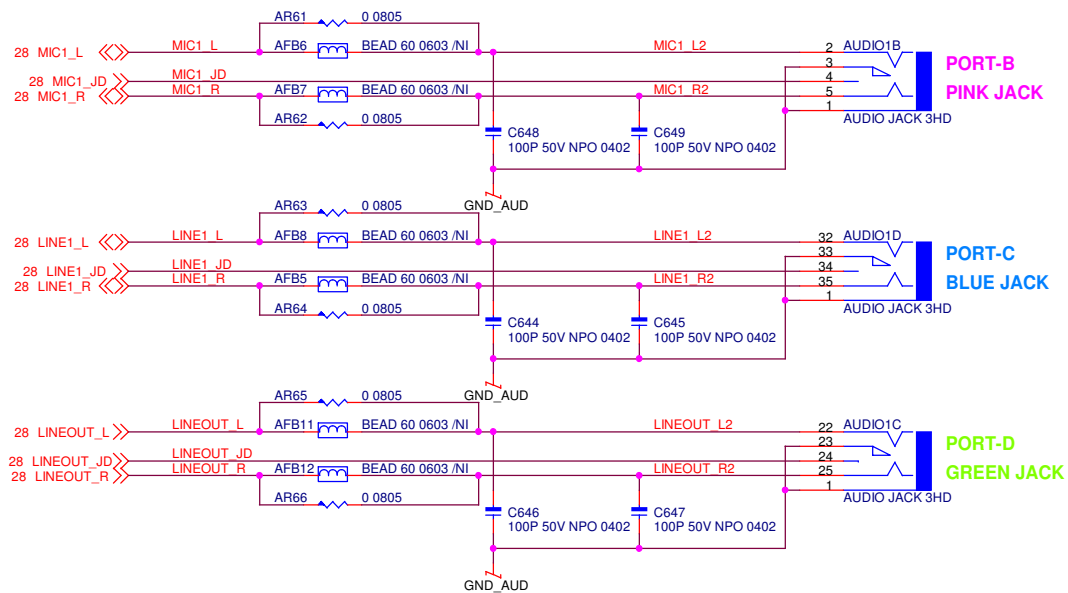
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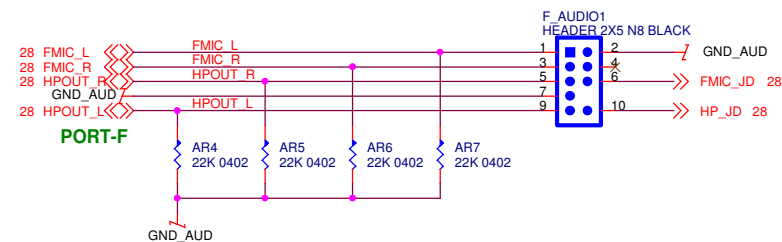
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(PAGE15/23/25/26/28/30/31/32/33)



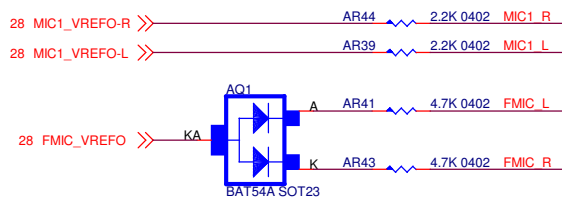




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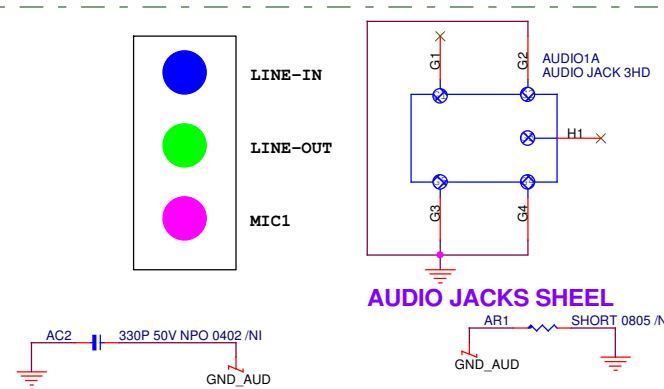


MIC VREF



SPDIF CONNECTOR

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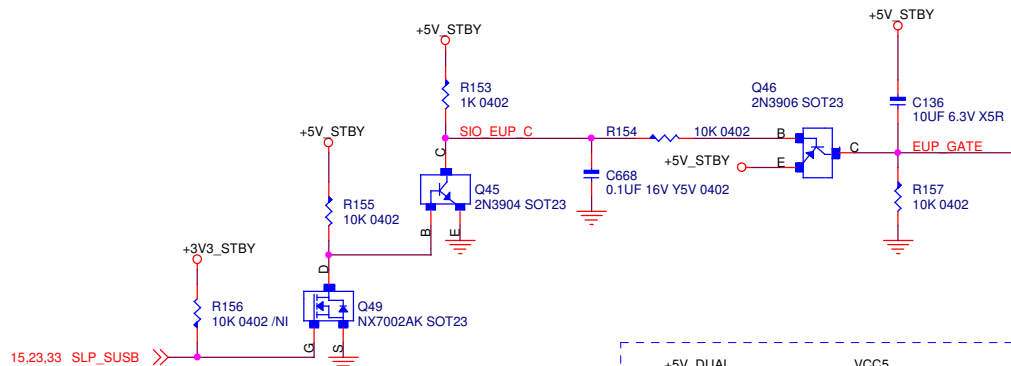


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AUDIO CONNECTOR

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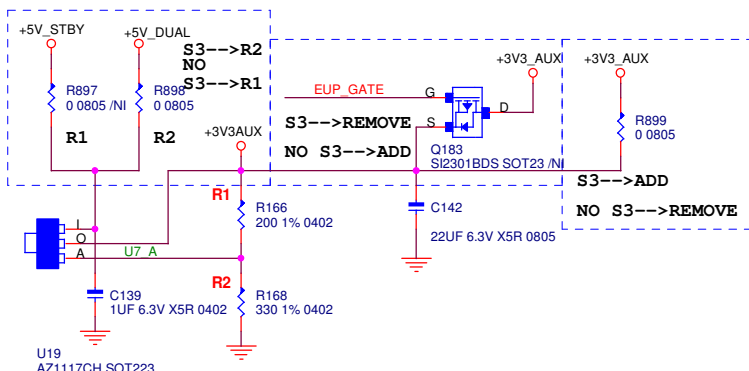
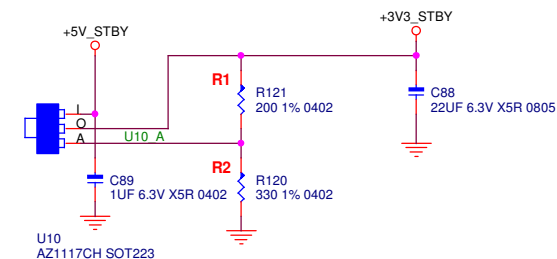
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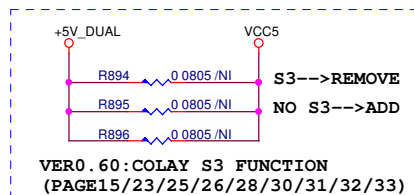
Energy-Using Product(EUP)

SLP_SUSB Hight :EUP OFF
SLP_SUSB Low :EUP ON

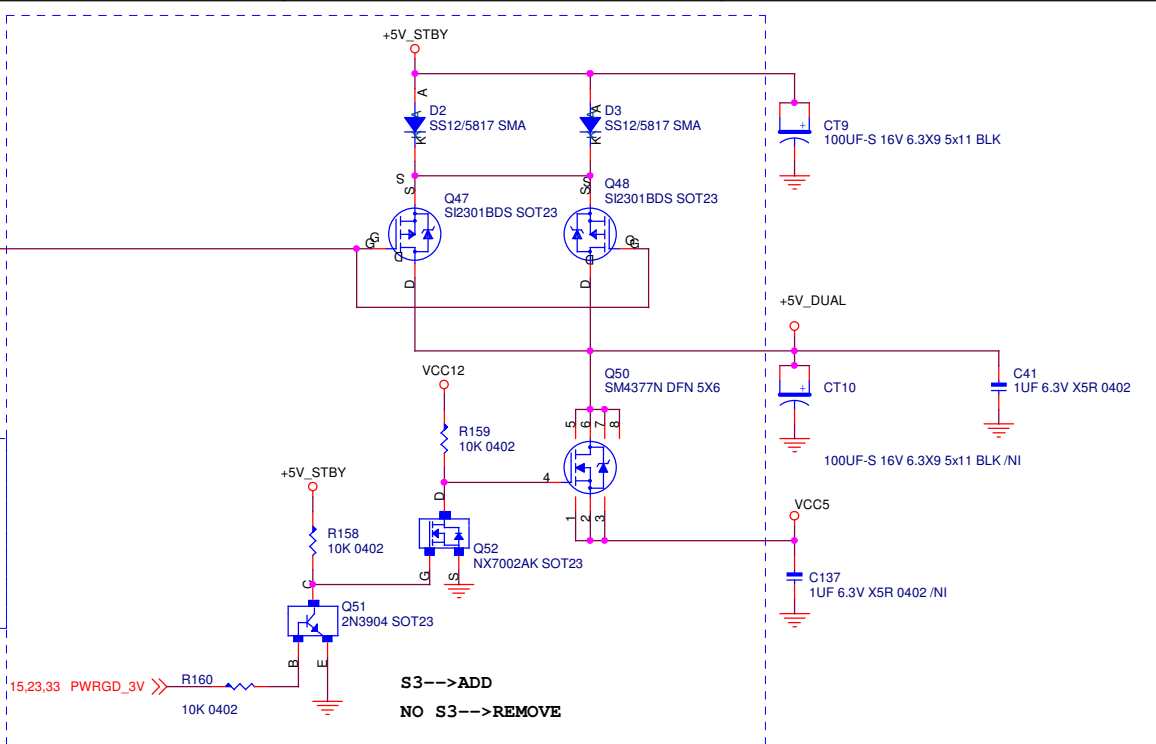
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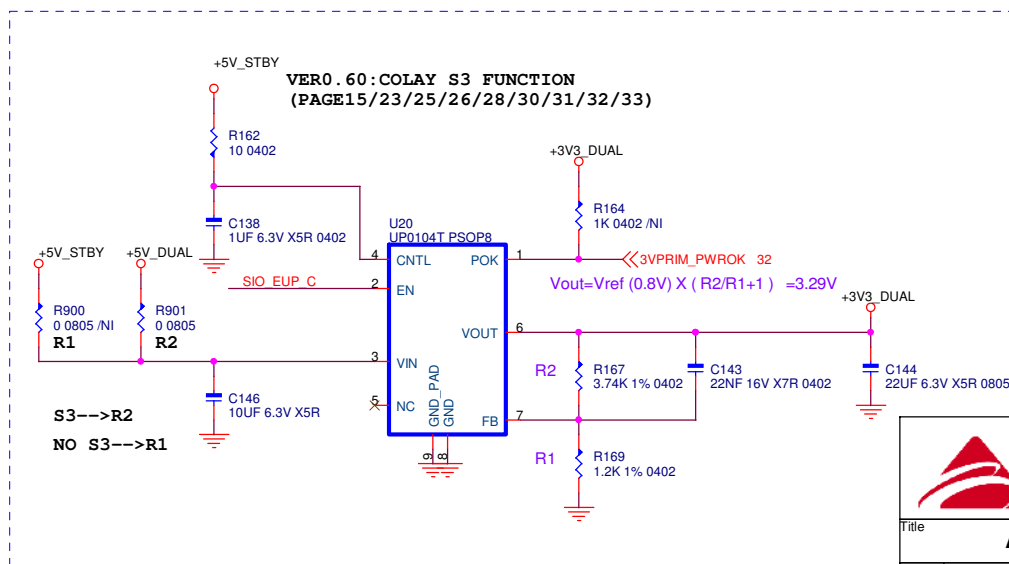
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VERO.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)



15,23,33 PWRGD_3V >> R160 10K 0402
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NO S3-->REMOVE



S3-->R2
NO S3-->R1

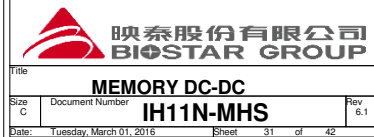
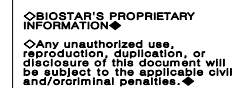
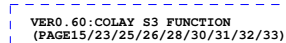
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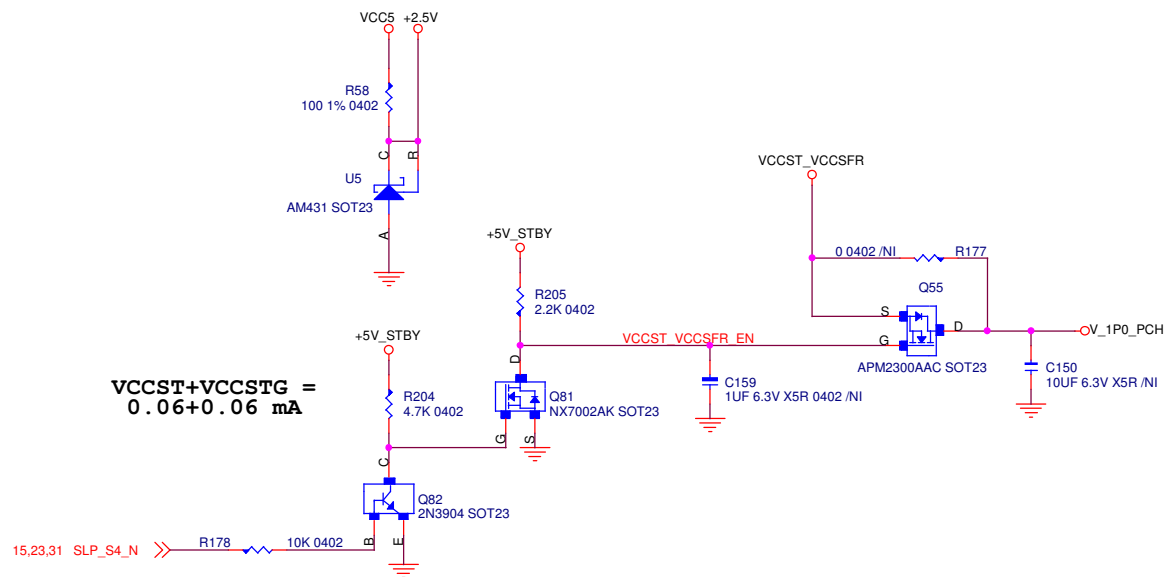
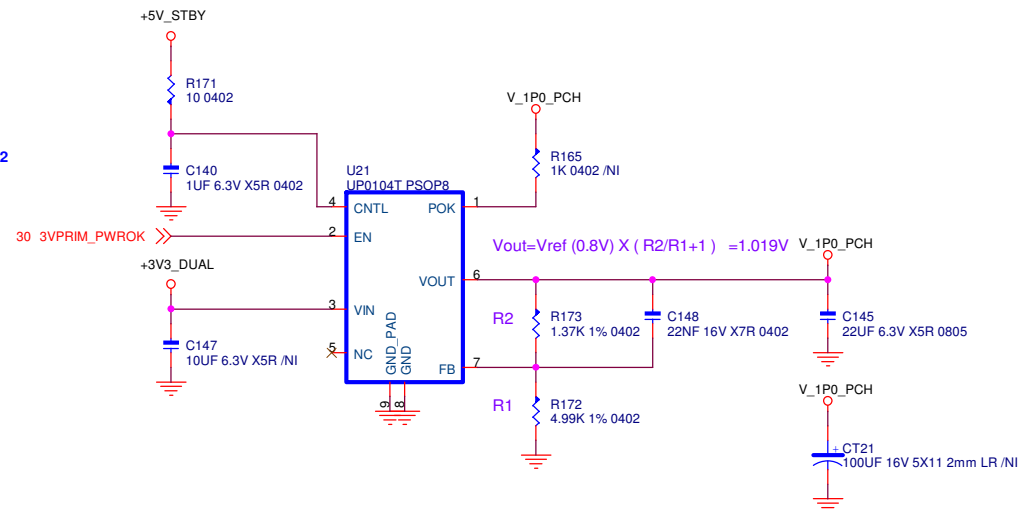
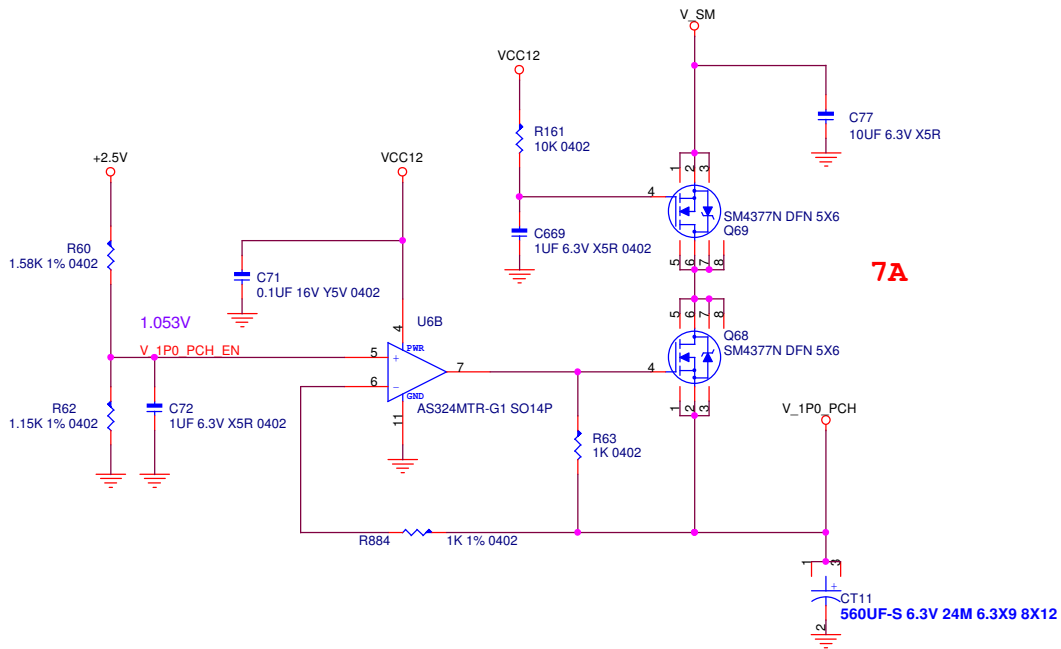
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VER0.60:COLAY S3 FUNCTION
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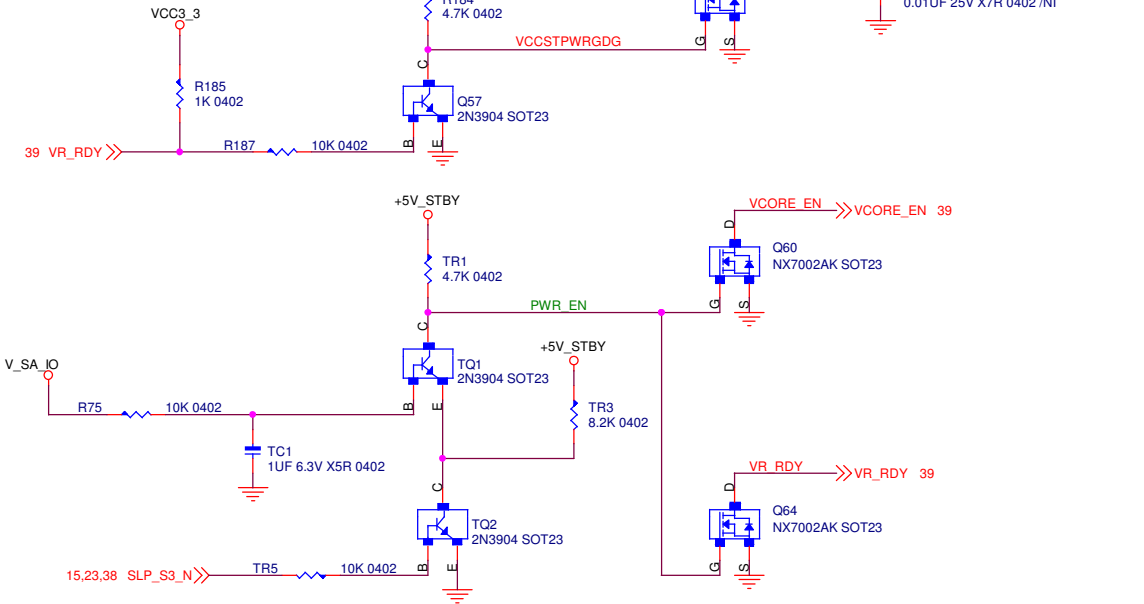
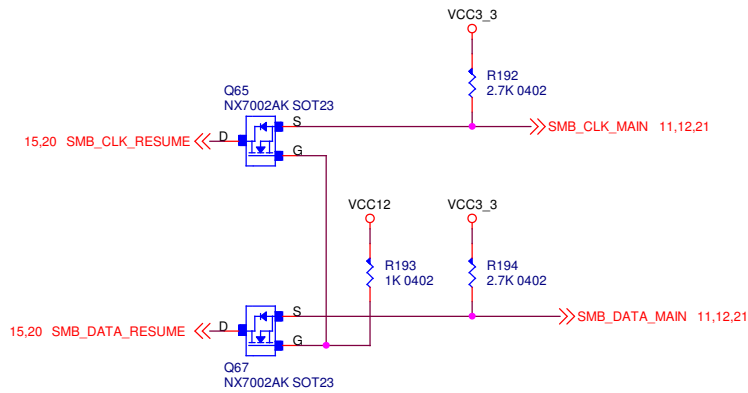
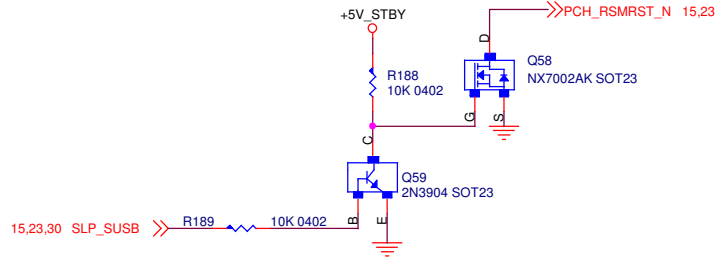
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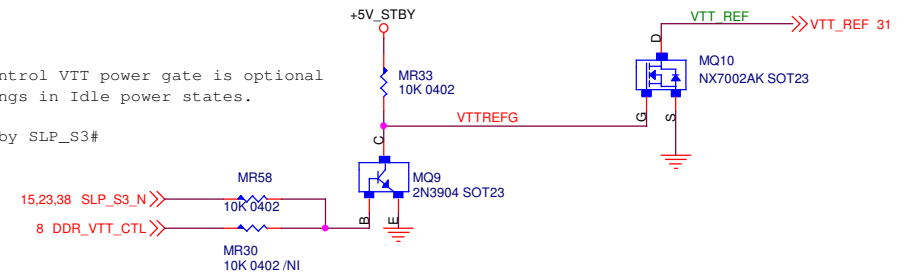
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39 VR_RDY >> VR_RDY R210 ISEN_SHORT /NI PCH_SYSPWROK >>PCH_SYSPWROK 15

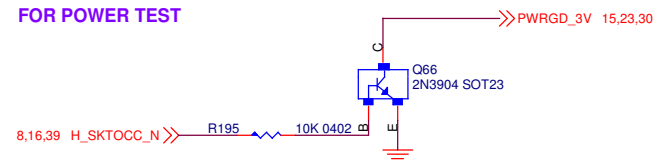
1.045V



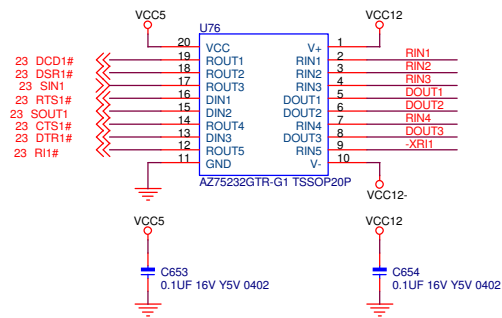
Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#



FOR POWER TEST



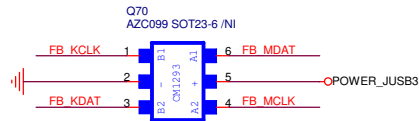
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COM PORT

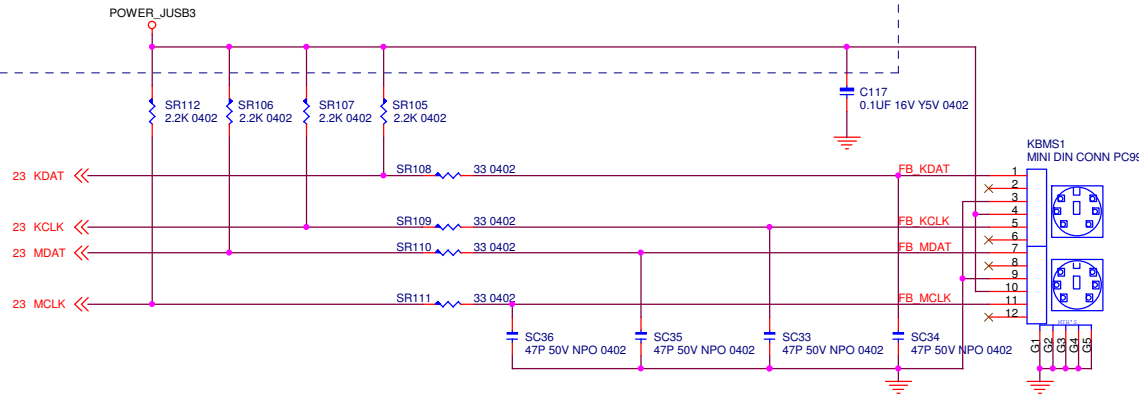
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WAKE ON RING



KEYBOARD & MOUSE

VER0.6: COST DOWN (POWER_JUSB4/POWER_JUSB5 COLAY) (PAGE25/34)



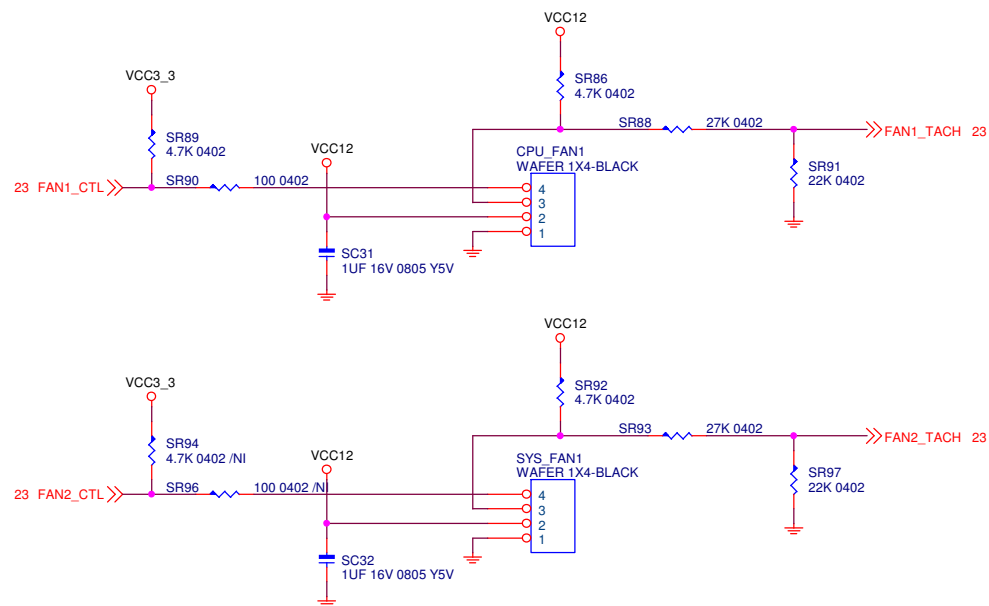
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COM1 / PS2 CONN

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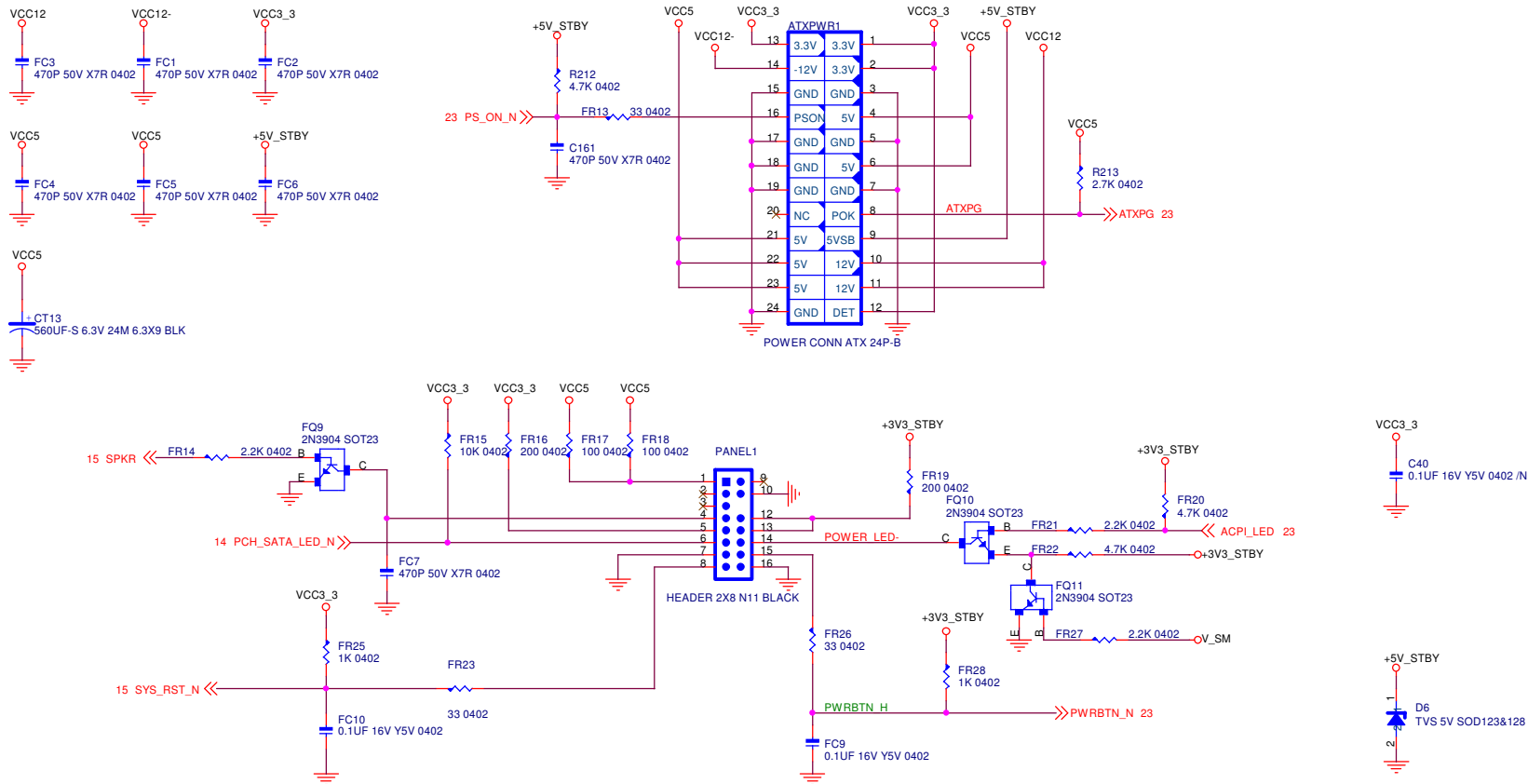
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FP PART: F+Reference

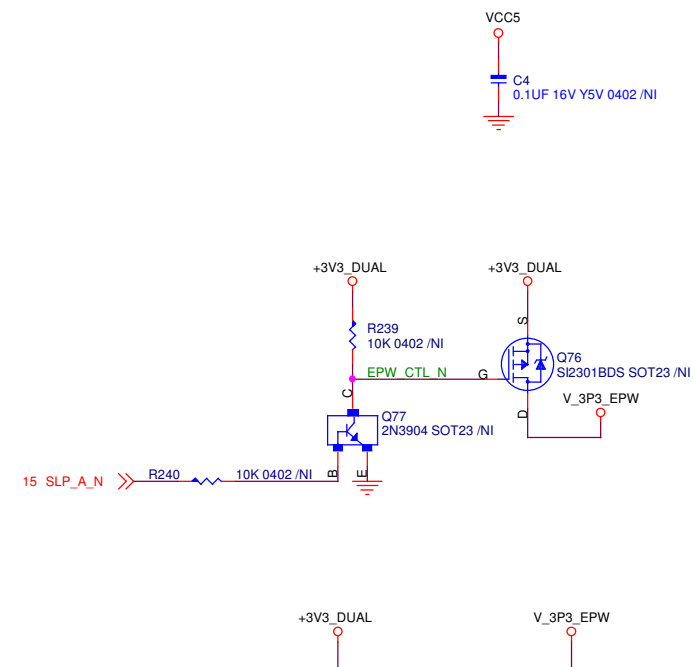
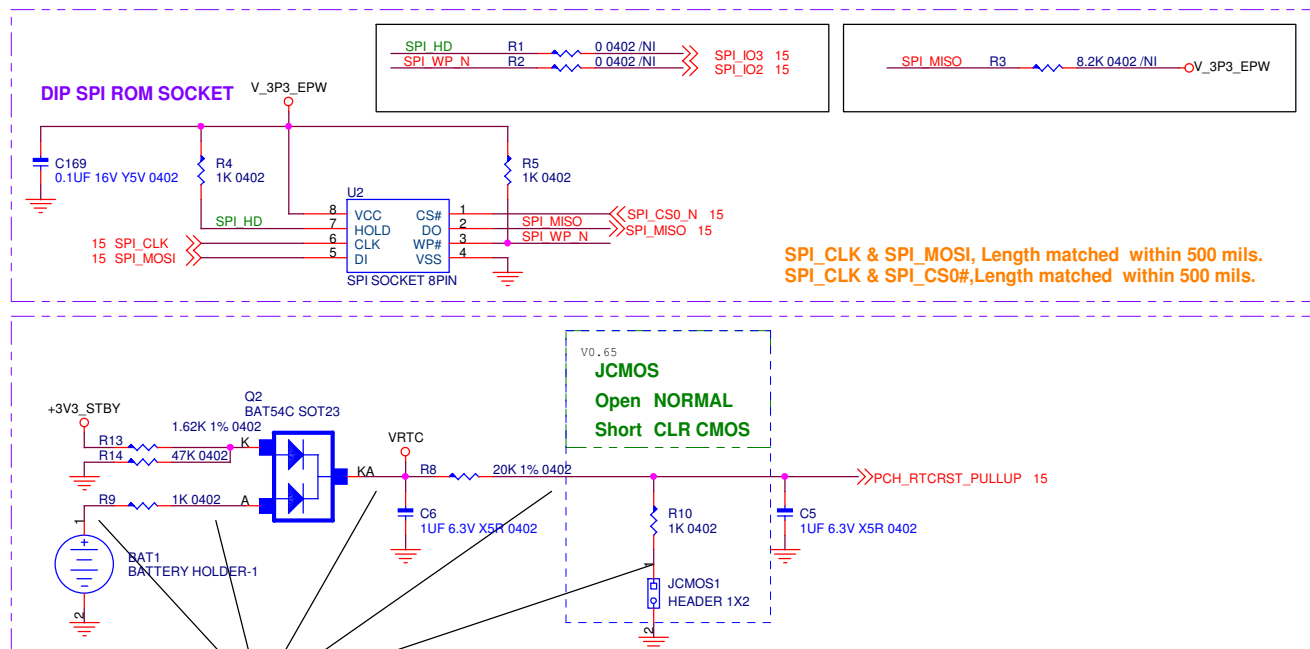


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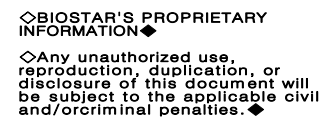
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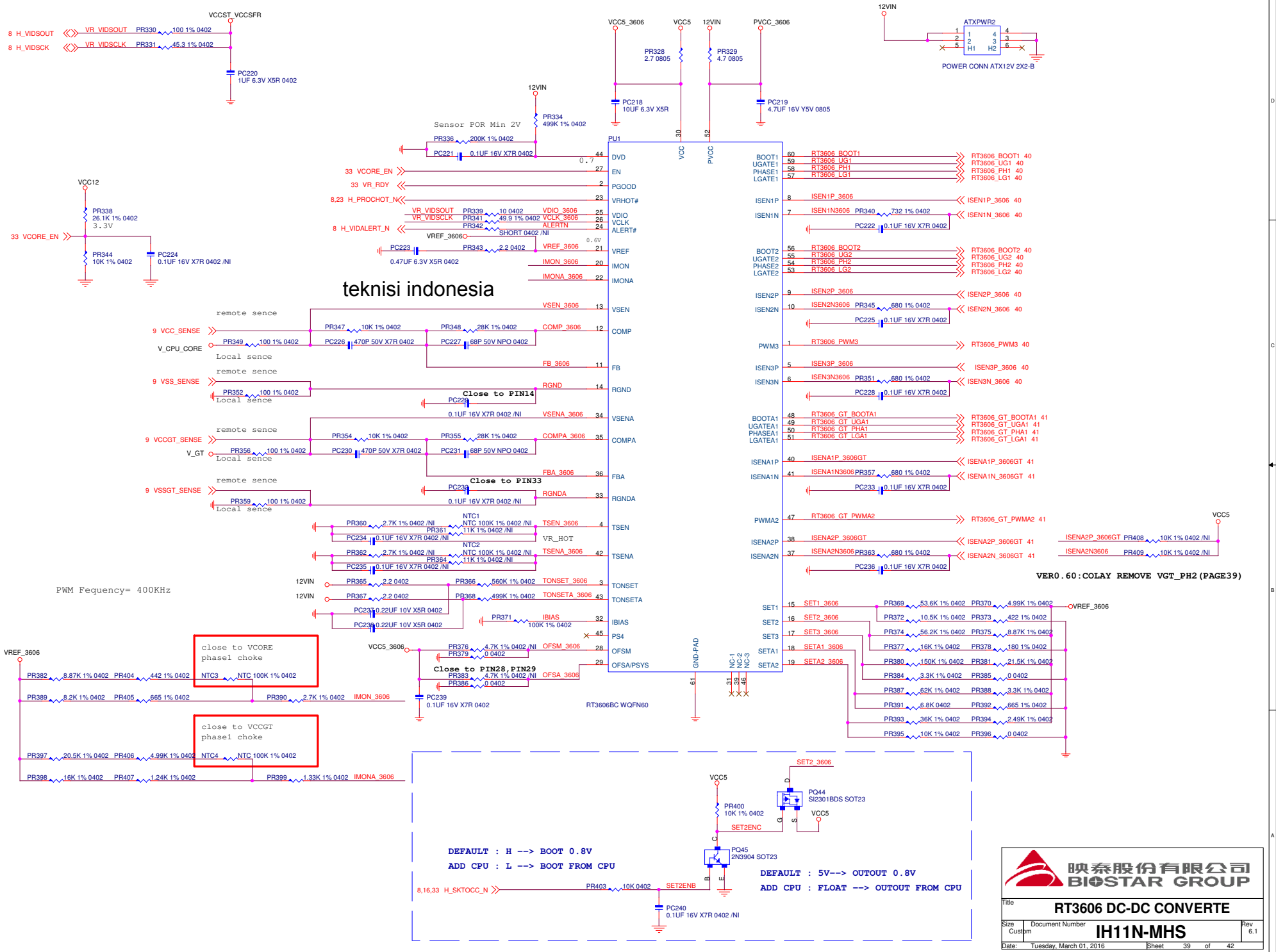
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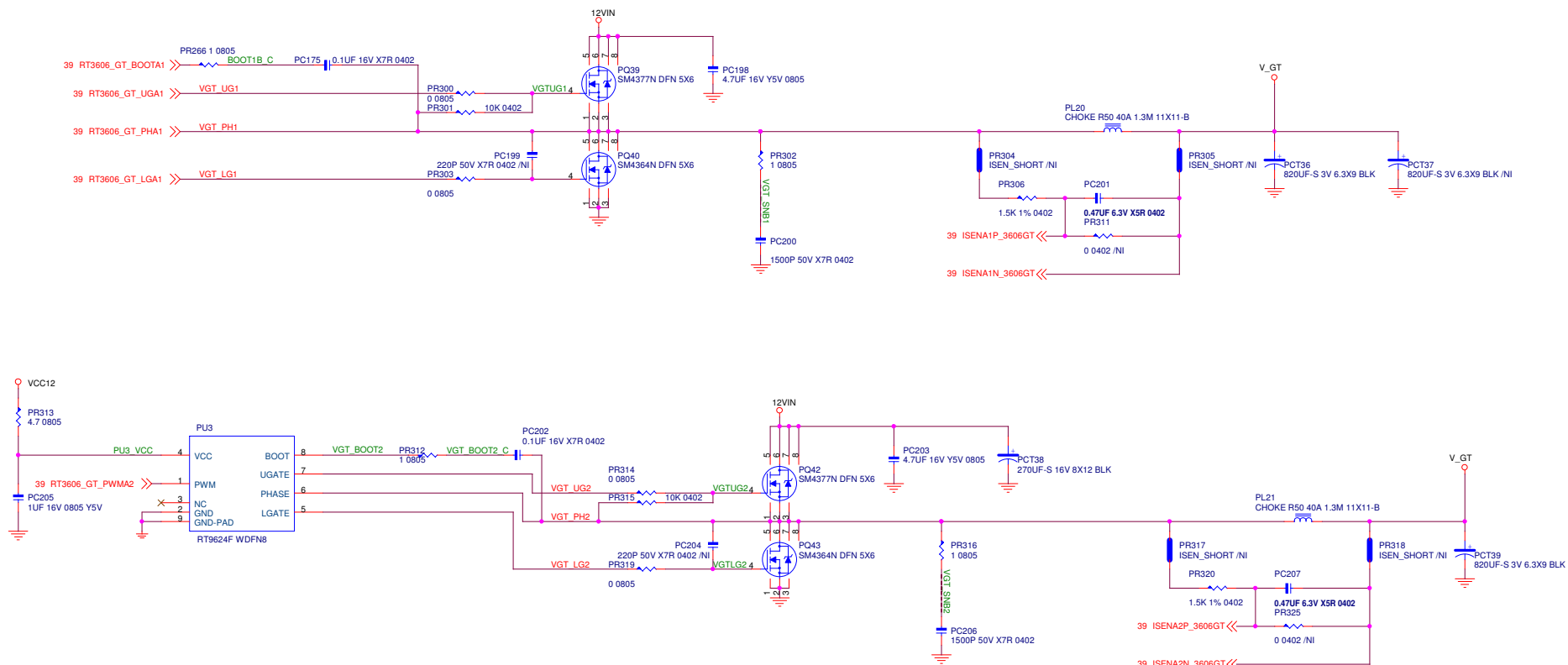
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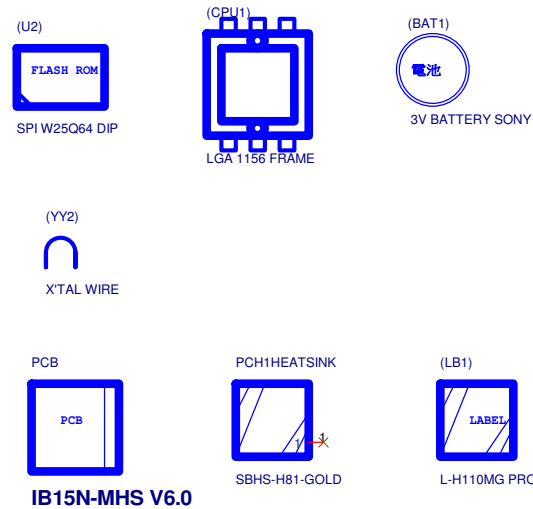
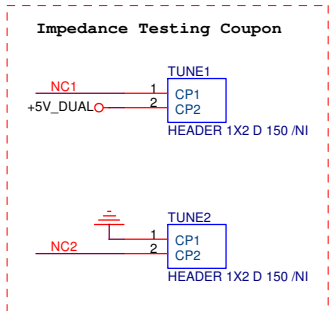
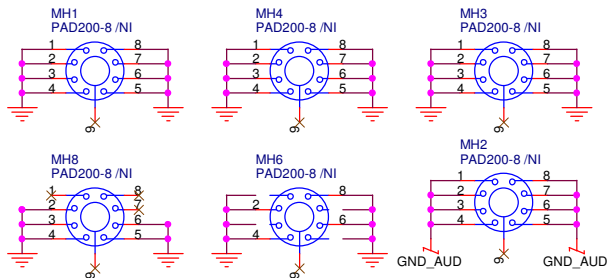





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